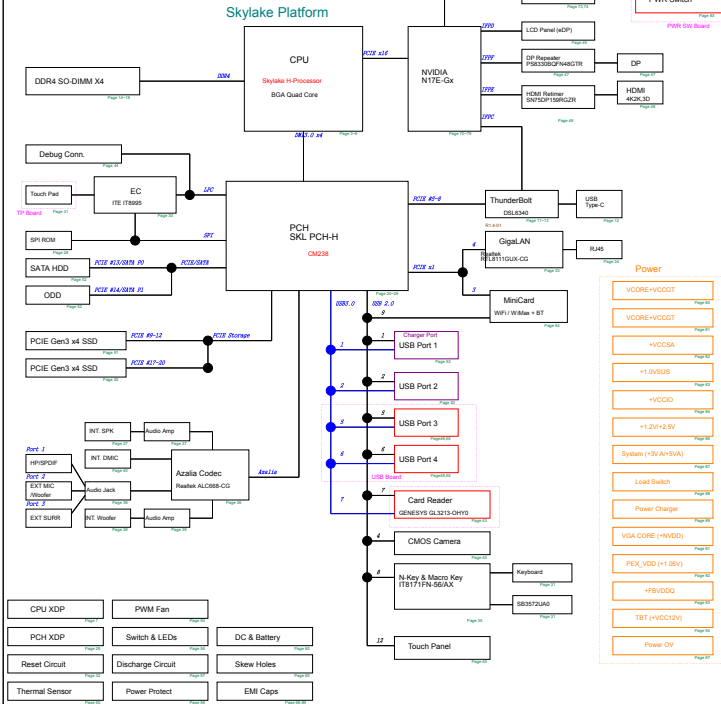
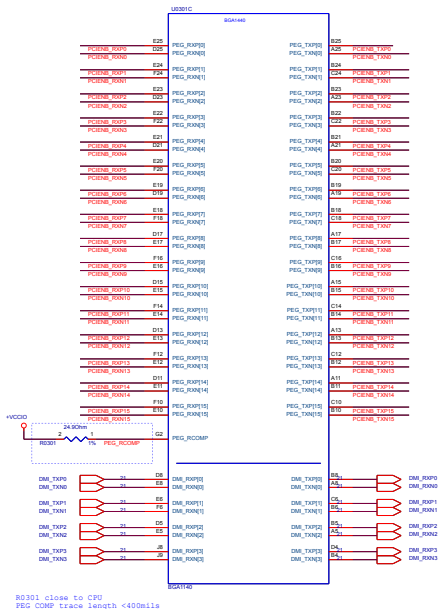


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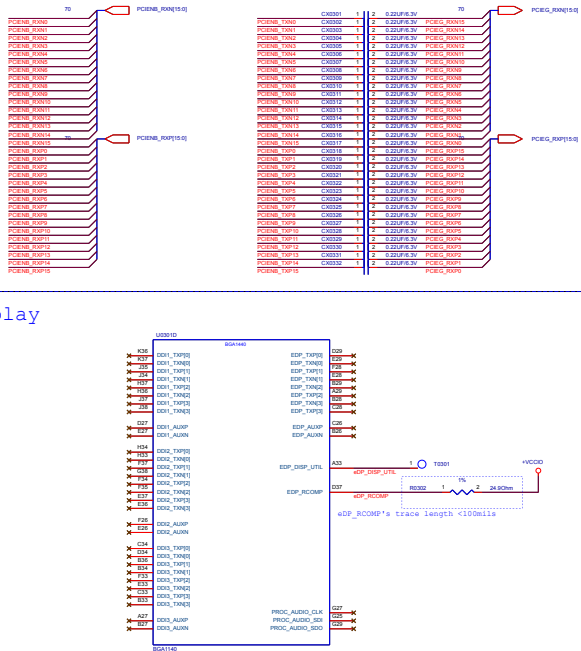
G752VSK Block Diagram



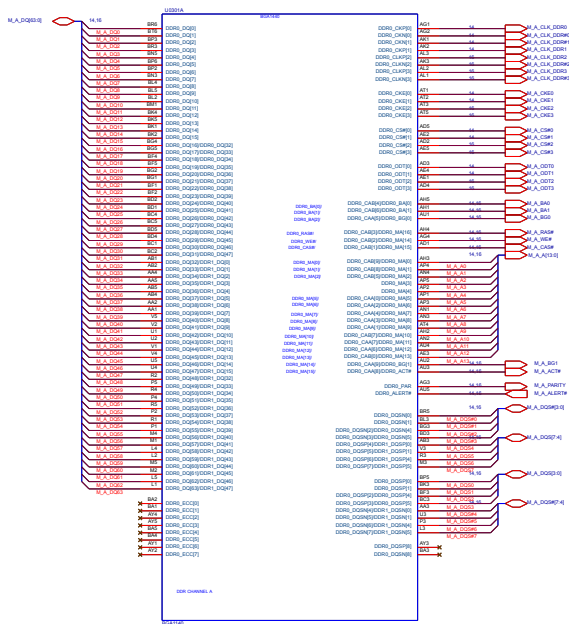
DMI & PCIEG



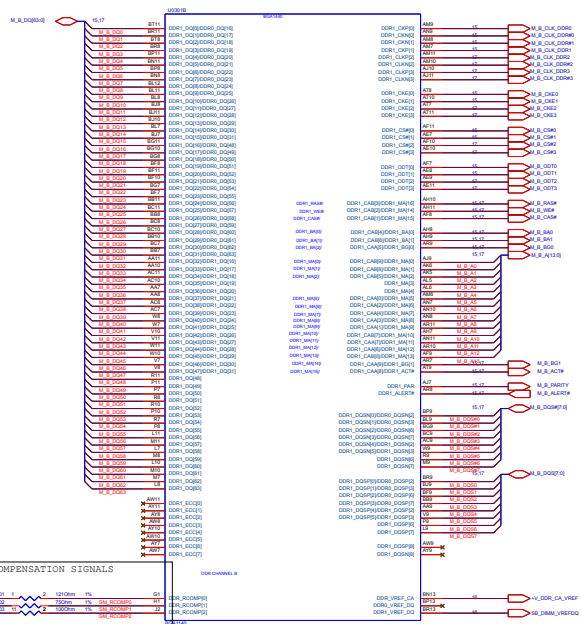
Display



Memory Channel A

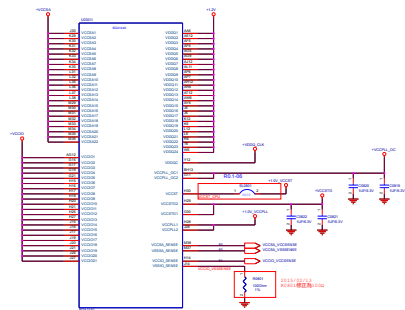


Memory Channel B



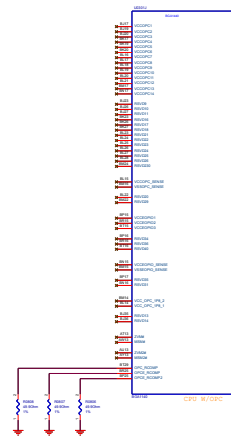
Main Board

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BGA1468			BGA1468			BGA1468		
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Y4	V55444	V55367	C13	V55286	V55261	B8B	V55148	V55687
Y5	V55443	V55366	C9	V55285	V55260	B8C	V55146	V55686
Y6	V55442	V55365	B126	V55282	V55259	B8D	V55144	V55683
Y10	V55441	V55364	B124	V55281	V55258	B8E	V55139	V55682
Y11	V55440	V55363	B122	V55280	V55256	B8F	V55138	V55686
Y5	V55448	V55362	B118	V55279	V55256	B8I	V55137	V55685
Y5A	V55447	V55361	B116	V55278	V55255	B8J	V55136	V55684
Y7	V55446	V55360	B114	V55277	V55253	B8K	V55135	V55681
W39	V55437	V55358	B10	V55276	V55252	B8L	V55143	V55680
W33	V55436	V55357	B106	V55274	V55251	B8M	V55141	V55677
W12	V55433	V55359	B105	V55273	V55250	B8N	V55140	V55676
W4	V55438	V55358	B104	V55272	V55249	B8P	V55139	V55675
W3	V55438	V55357	B103	V55271	V55248	B8Q	V55138	V55674
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W3	V55248	V55248	B8	V55176	V55153	B8K	V55040	V55579
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W3	V55216	V55216	B0	V55160	V55137	B8B	V55024	V55563
W3	V55214	V55214	B0	V55159	V55136	B8C	V55023	V55562
W3	V55212	V55212	B0	V55158	V55135	B8D	V55022	V55561
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W3	V55208	V55208	B0	V55156	V55133	B8F	V55020	V55559
W3	V55206	V55206	B0	V55155	V55132	B8G	V55019	V55558
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W3	V55198	V55198	B0	V55151	V55128	B8K	V55015	V55554
W3	V55196	V55196	B0	V55150	V55127	B8L	V55014	V55553
W3	V55194	V55194	B0	V55149	V55126	B8M	V55013	V55552
W3	V55192	V55192	B0	V55148	V55125	B8N	V55012	V55551
W3	V55190	V55190	B0	V55147	V55124	B8P	V55011	V55550
W3	V55188	V55188	B0	V55146	V55123	B8Q	V55010	V55549
W3	V55186	V55186	B0	V55145	V55122	B8R	V55009	V55548
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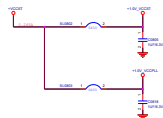


OPC Power Rails

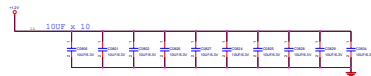
Main Board



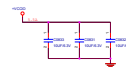
+1.0V_VDDQST/+1.0V_VDDQPL
DECAPS Place Back Side (TOP)



+VDDQ DECAPS Place Back Side (TOP)



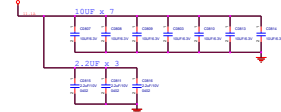
+VCCIO DECAPS Place Back Side (TOP)



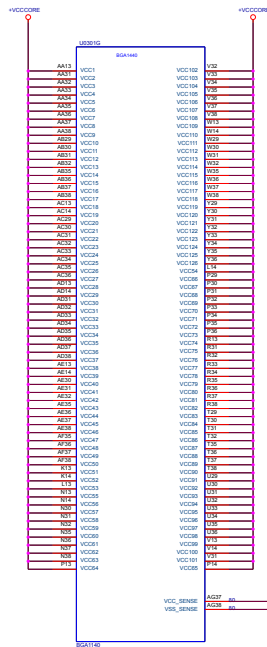
+VDDQ_CLK DECAPS Place Back Side (TOP)



+VCCSA DECAPS Place Back Side (TOP)



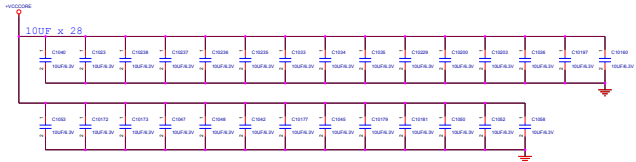
Voltage Segment
+VCCIO is supplied +1.0V2 (shared with +VCCSTG)



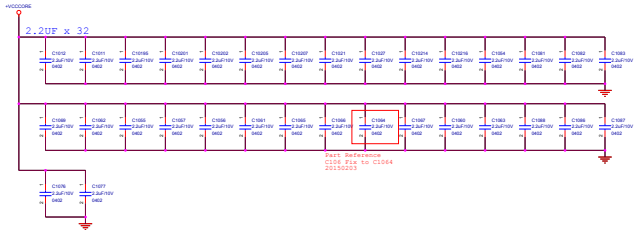
WWW.AliSaler.Com

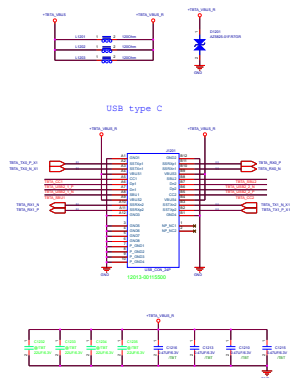
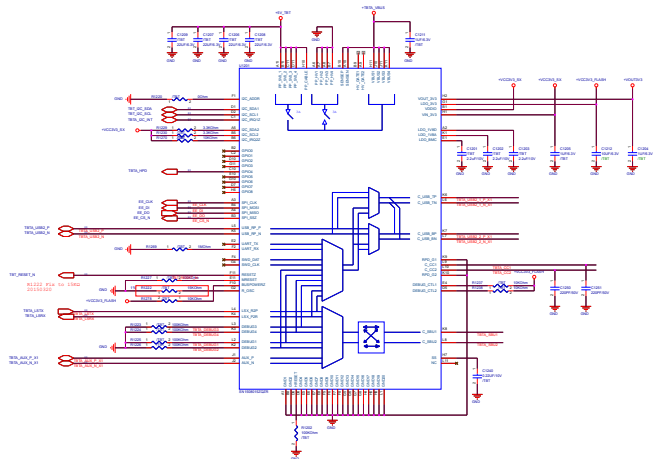
Main Board

+VCCORE DECAPS Place Back Side (TOP)

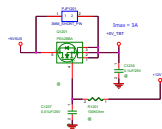


+VCCGT DECAPS Place Back Side (TOP)

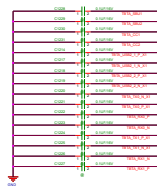




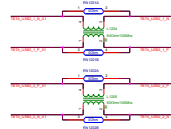
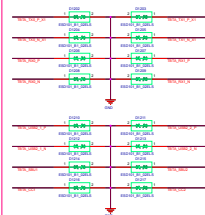
TBT 5V Power



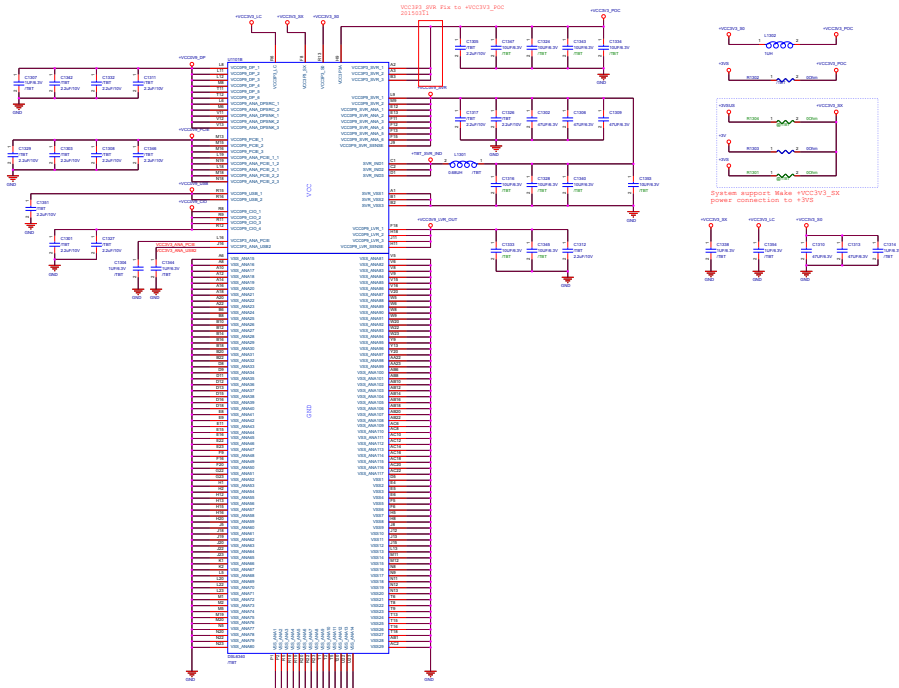
ESD-Protection



20161011 ADD ESD on high speed lines

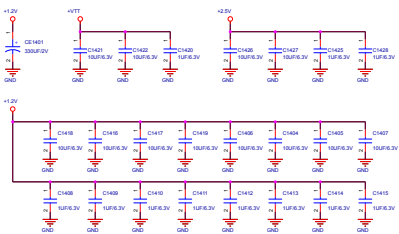
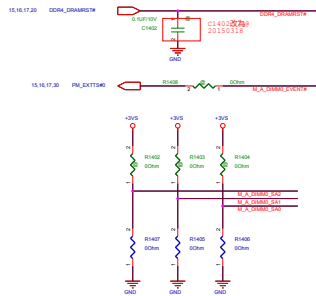
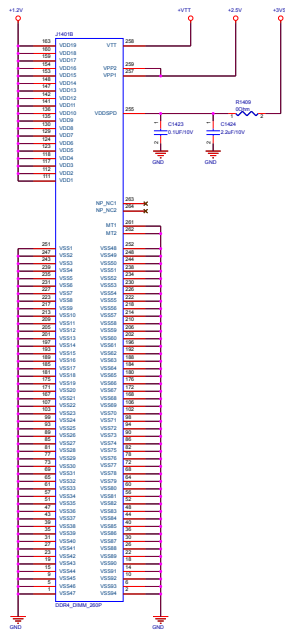
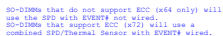


Main Board



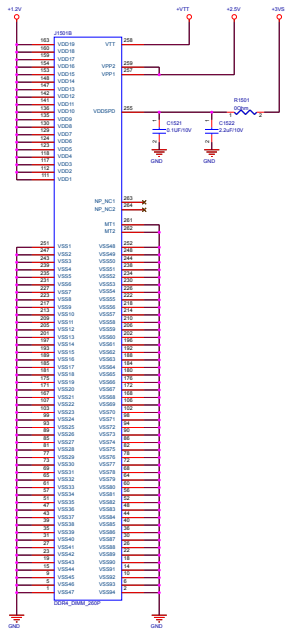
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12002-00080600
DDR4 DIMM 260P 4H REV



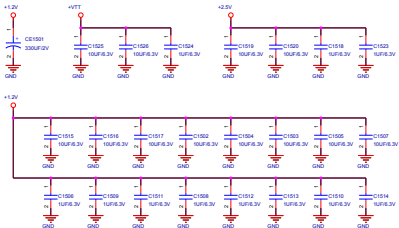
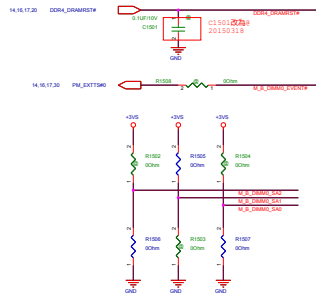
Main Source	1th FWR	2nd FWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From FUS600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

12002-00080700
DDR4 DIMM 260P 4H STD



SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENTS ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH



Main Source	1th FWR	2nd FWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From FU8600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSX	+3VS
		+2.5V

12002-00080700
DDR4 DIMM 260P 4H STD

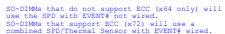
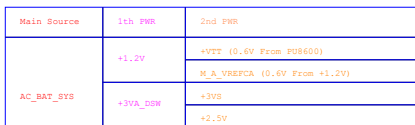
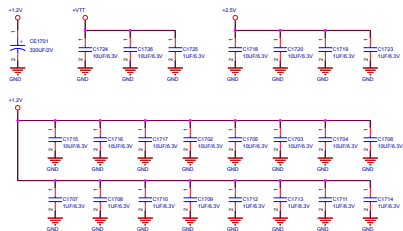
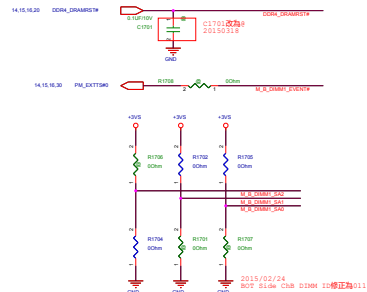
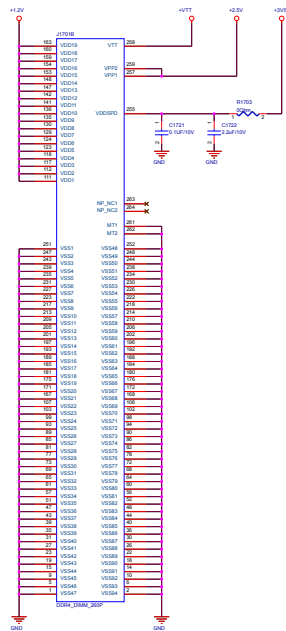
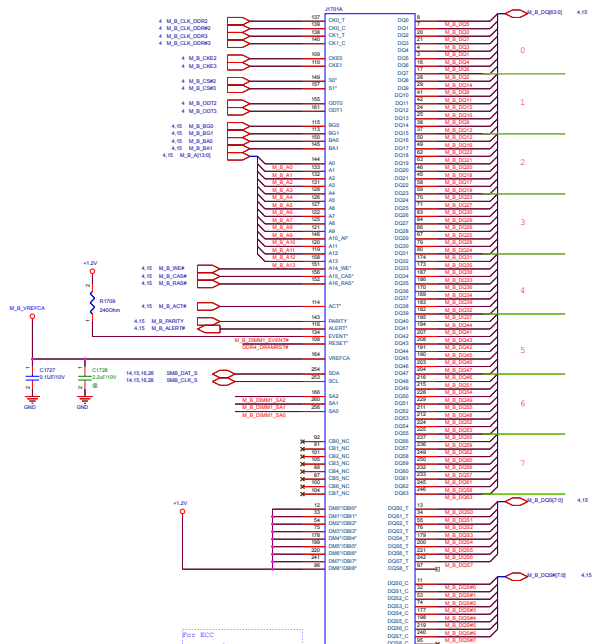


Figure 1: PCB layout of the DCR4-DRAM81W. The figure contains three sub-diagrams. The top diagram shows a power plane with a 5V100V net, a C1601 capacitor, and a GND connection. The middle diagram shows a signal trace for PA1_EXTIO0 with a 50ohm termination and a 100ohm series resistor. The bottom diagram shows a multi-layer PCB layout with three vertical signal traces connected to +3V5 and GND, with various resistors (R1800, R1803, R1804, R1802, R1805, R1807) and capacitors (C1601, C1602, C1603) labeled.



12002-00080500
DDR4 DIMM 260P 8H STD



Main Source	1th FWR	2nd FWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From FU5600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSM	+3VS
		+2.5V

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SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.

SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN BCH

The diagram illustrates the electrical connection between a SKL-H/S processor and a DDR3L SO-DIMM module. The processor's **DDR1_VREF_DQ** and **DDR1_VREF_CA** pins are connected to the **VREF_DQ** and **VREF_CA** pins of the DIMM connectors. The DIMM module is labeled **DDR3L SO-DIMM** and shows two channels, Channel 0 and Channel 1, each with **VREF_DQ** and **VREF_CA** pins. The module is powered by **VCCM** and **VCC** pins, with decoupling capacitors (22 nF, 25 nF, 18 nF, 15 nF) shown. The module is labeled **DDR3L SO-DIMM**.

The schematic diagram illustrates the SB_DMM_VREFDQ circuit. It features a differential signal path. At the top, a 1.2V supply is connected to a 1% 180Ω resistor (R1811). This resistor is connected to a node labeled "1% 180Ωm". This node is connected to a 2.2Ω resistor (R1809), which is connected to a node labeled "2.2Ωm". This node is connected to a 1% 180Ω resistor (R1812), which is connected to a node labeled "1% 180Ωm". This node is connected to a 24.90Ω resistor (R1808), which is connected to a node labeled "24.90Ωm". This node is connected to a 0.022μF/16V capacitor (C1802), which is connected to a node labeled "0.022μF/16V". This node is connected to a 0.1μF/16V capacitor (C1808), which is connected to a node labeled "0.1μF/16V". This node is connected to a 0.1μF/16V capacitor (C1809), which is connected to a node labeled "0.1μF/16V". The circuit is grounded at multiple points, including a common ground and individual grounds for the capacitors.

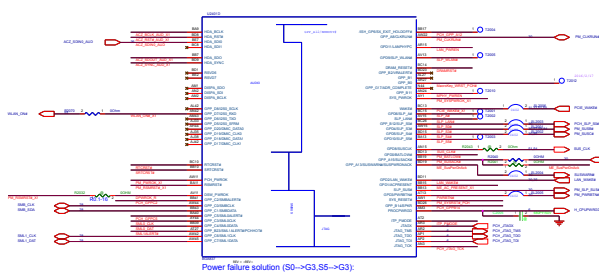
AC2_BCLR_A0 1 JTAG1
 AC2_FVNC_A0 2 JTAG2
 AC2_FVNC_A1 3 JTAG3
 AC2_B0CNT_A0 4 JTAG4

NDA_JTAG[On-Die JTAG voltage select]:
 NDA_Tap edge of 3000000000 pin
 High:1.5V, Low:1.0V (default)

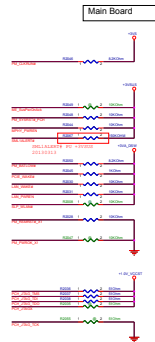


```
ACE SDOOT:
(1)PCW:
Internal PD 20k ohm,
VIL<0.35V,VIH>0.65-1.3V
(2)ALC149:
VIL<0.35+1.3V,VIH>0.65+1.3V
```

ACI HIGH is a signal used for Flash Descriptor security Override/DE debug mode
HIGH : get overrides, LOW : disable override



Power failure solution (S0→G3,S5→G3):



Main Source	1st FWS	2nd FWS	3rd FWS	4th
WETZBET	<WETZ_BET	<WETZ_BET		
AC_BAT_210	<+_V000B	<V002T	<+1_0V_V003T	
	<+1_2V			
	<V006	<V006	<V006_BCT	
	<+V08_20W	<+V002B	<+V002B_FCH	<V00CA210
		<+V02		



PCB_GPCB: with internal pull down	
PU	02PI
PD	LPC (default)



PC_CPCCI: weak internal pull down	
PU	Enable
PD	Disable (default)



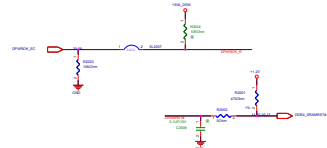
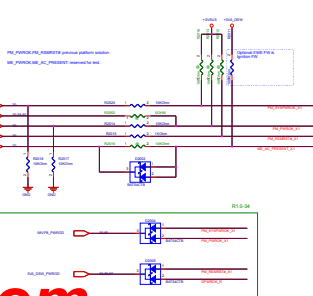
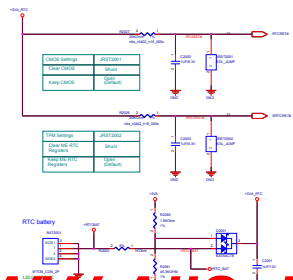
PCA_CFR01: weak internal pull down	
PU	Enable
PD	Disable (Default)

Figure 1: Schematic representation of the 1000 Genomes Project. The diagram shows a network of 26 populations (labeled 1-26) connected by lines representing genetic relationships. A central box labeled '1000 Genomes Project' is connected to all populations. The populations are grouped into five clusters: African (1-5), European (6-10), Asian (11-15), Admixed American (16-20), and Other (21-26).

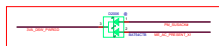
Boundary Scan TP (PCH) R0.1-37

PCH Pin	Signal	R0.1-37 Pin	Signal
T2607	PCH_T2607_T2607	T2607	T2607
T2608	PCH_T2608_T2608	T2611	T2611
T2609	PCH_T2609_T2609	T2613	PCH_T2613_T2613
T2610	PCH_T2610_T2610	T2615	T2615
T2614	PCH_T2614_T2614	T2615	PCH_T2615_T2615

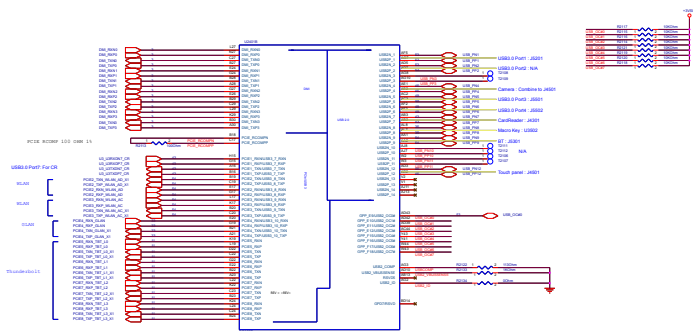
HKG2_PCH



SPCH10	POH	PLT	1	us	POH_PWRK low to VCCIO dropping 5% of nominal value
SPCH12	POH	PLT	1	us	RMRST# asserting to VccPRST dropping 5% of nominal value
SPCH14	POH	PLT	1	us	DSW_PWRK falling to any of VccDSW; VccHistry dropping 5% of nominal value

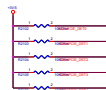
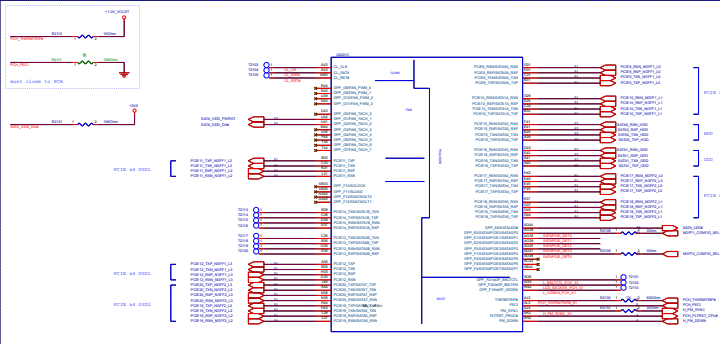


SKL, PCH-H C236				SKL, G751VC PCIe CLK Define			
HSIO Detail		Function		PCIe CLK SRC		Function	
0	PCI02 (From CPU)		iGPU			SRC0	
1	USB3 #1		USB I/O(USB3_0)				
2	USB3 #2	SSIC #1					
3	USB3 #3	SSIC #2					
4	USB3 #4						
5	USB3 #5		USB I/O(USB3_2)				
6	USB3 #6		USB I/O(USB3_3)				
7	USB3 #7	PCIe #1				SRC1	
8	USB3 #8	PCIe #2					
9	USB3 #9	PCIe #3				SRC3	
10	USB3 #10	PCIe #4	QoS			SRC4	
11	PCIe #5	QoS					
12	PCIe #6						
13	PCIe #7						
14	PCIe #8						
15	PCIe #9	SATA #0	QoS				
16	PCIe #10	SATA #1					
17	PCIe #11						
18	PCIe #12	QoS					
19	PCIe #13	SATA #0*	QoS				
20	PCIe #14	SATA #1*					
21	PCIe #15	SATA #2					
22	PCIe #16	SATA #3					
23	PCIe #17	SATA #4					
24	PCIe #18	SATA #5					
25	PCIe #19	SATA #6					
26	PCIe #20	SATA #7					

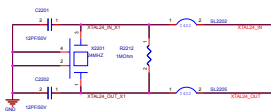


USB Setting

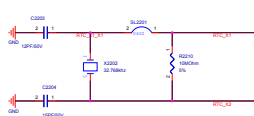
SKL, G751VC USB2 & USB3 Define			
USB2	Function	USB2	Function
USB2 #1	USB I/O(USB3_0)	USB2 #1	USB I/O(USB3_0)
USB2 #2		USB2 #2	
USB2 #3		USB2 #3	
USB2 #4	Camera	USB2 #4	3D Camera
USB2 #5	USB I/O(USB3_2)	USB2 #5	USB I/O(USB3_2)
USB2 #6	USB I/O(USB3_3)	USB2 #6	USB I/O(USB3_3)
USB2 #7	USB Card Reader	USB2 #7	USB Card Reader
USB2 #8	Macro Key	USB2 #8	
USB2 #9	BT	USB2 #9	
USB2 #10		USB2 #10	
USB2 #11			
USB2 #12	Touch Panel		
USB2 #13			
USB2 #14			



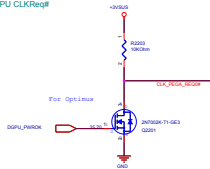
XTAL 24MHz



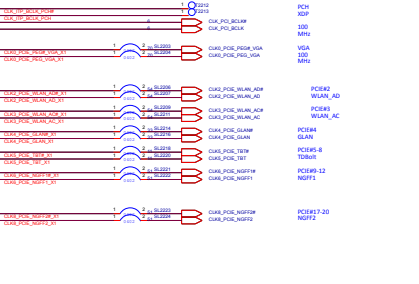
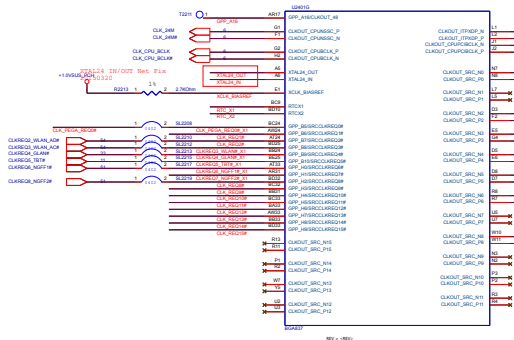
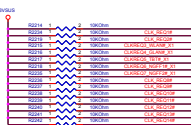
RTC CRYSTAL 32.768KHz



DGPU CLKReq#



PCH CLKREQ Setting:

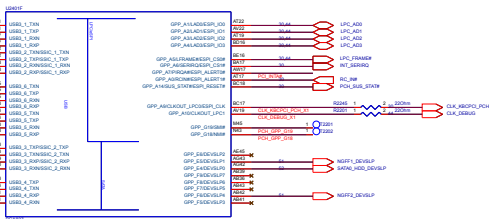


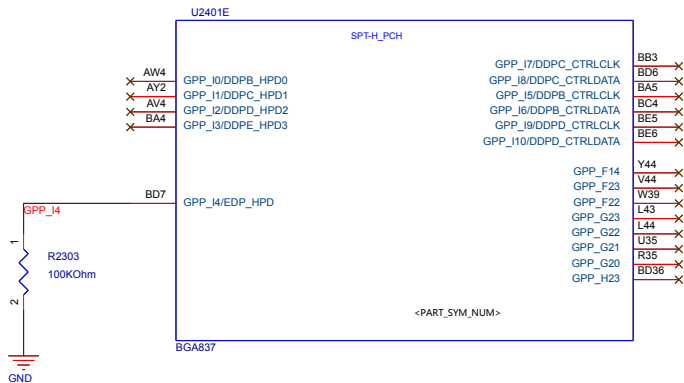
USB10 Port1 : J5001

USB10 Port2 : N/A

USB10 Port4 : J5002


USB10 Port3 : J5001



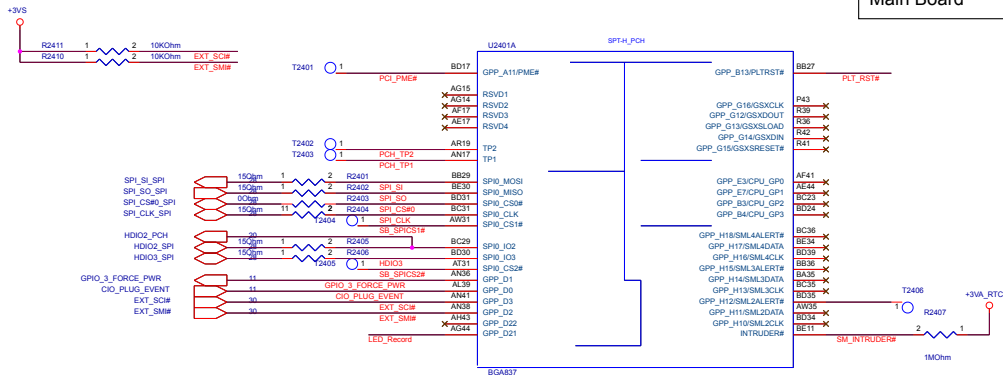


DDPD Strap Setting Update :
 0 = Port D is not detected (Default)
 1 = Port D is detected
 20150309

REV = <REV>

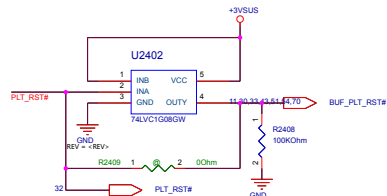
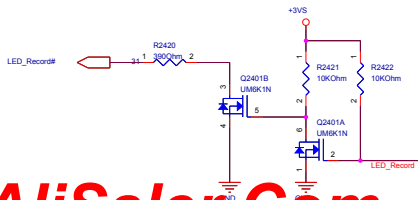
		Project Name	Rev
		G752VSK	R2.0
Title : PCH-CPT(4)_C801,PCI,DP			
Size	Dept.:	Engineer:	
A	ASUSTeK COMPUTER INC.	Ashton_yang	
Date:	Wednesday, October 12, 2016	Sheet	23 of 102

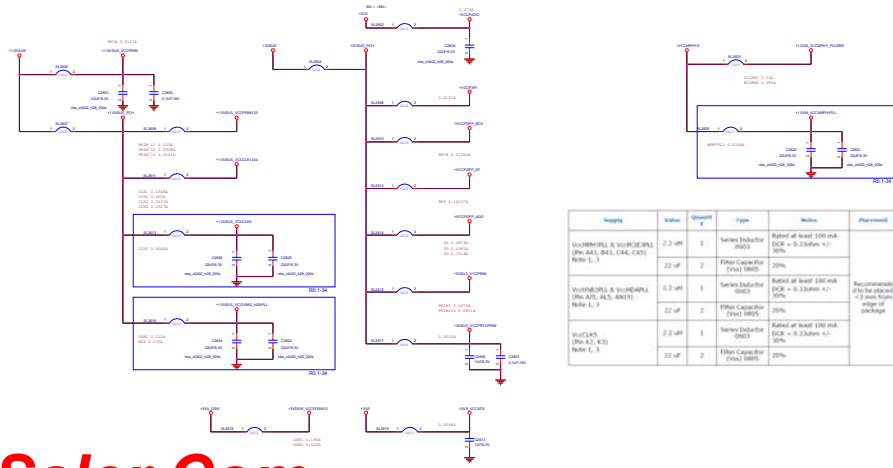
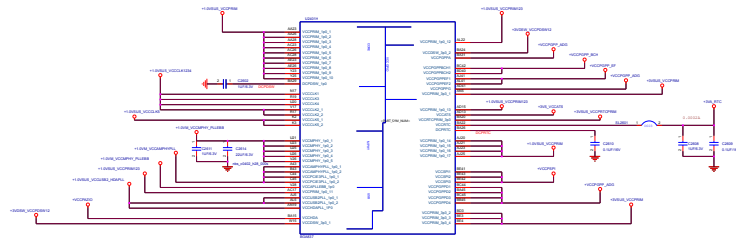
Main Board



Record Key LED Control Circuit

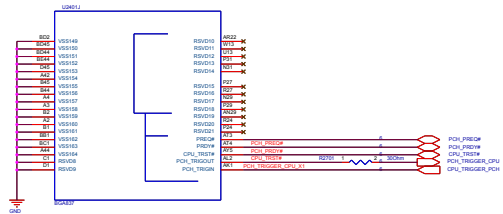
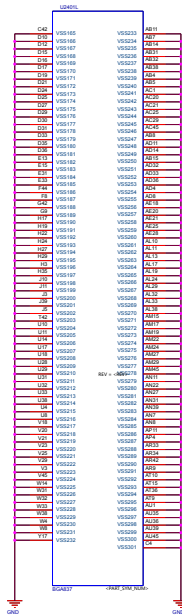
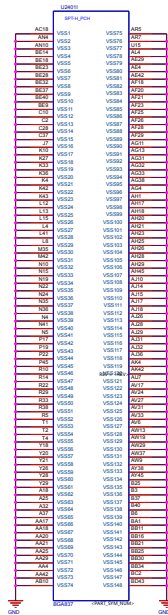
LED Record# of Current :
 $(5 - 2.35) / 390 = 6.8\text{mA}$





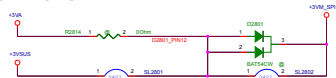
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Main Board



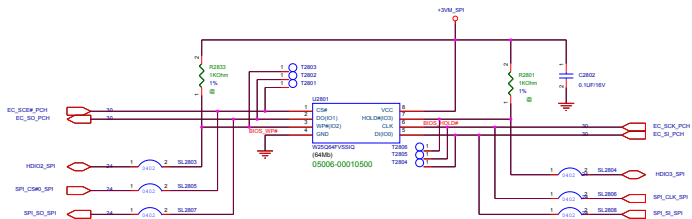
Main Board

SPI Power

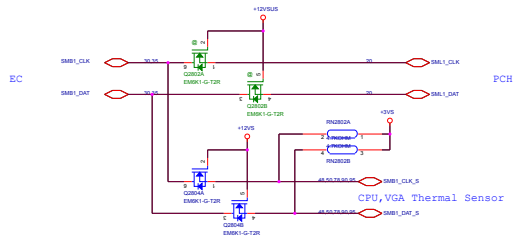


1st SPI ROM

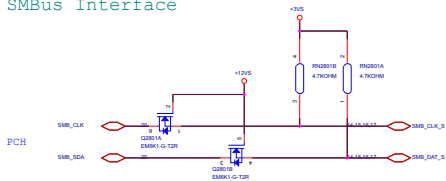
Main: 05006-00010500 (fixed quad bit)



System Management Interface

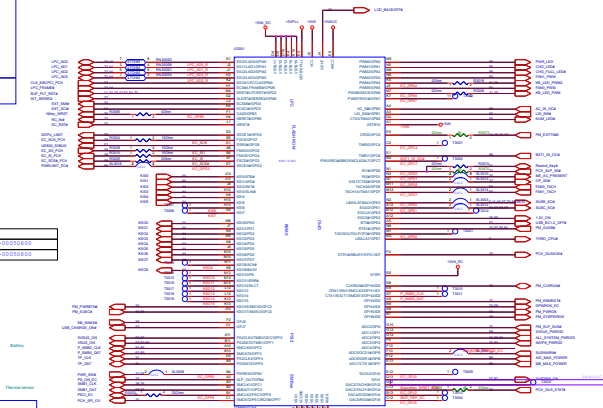
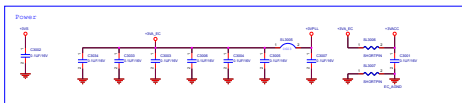


SMBus Interface



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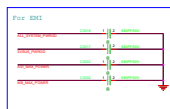
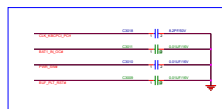
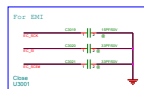
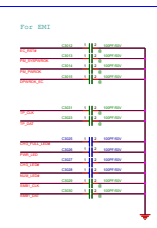
EC 8995
Only 3V Tolerance GP2[0,1,2,3,4,5,6] GP2[3,4,5,6,7] GP2[0,4,6,7] GP2[6] GP2[7] GP2[0,17] GP2[0,7]
Can be adjusted to Open-drain for pull
GP20-GP23 GP20-GP27 GP20-GP27 GP20-GP27 GP20-GP27 GP20-GP26 GP20-GP23
EC Impulse



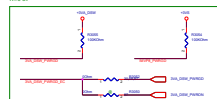
EC Version	ADIS 9/5
17889500-128/24	880377-00000000
17889500-128/24	880377-00000000

Safety

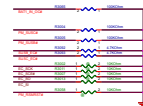
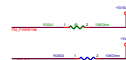
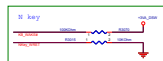
Thermal sensor

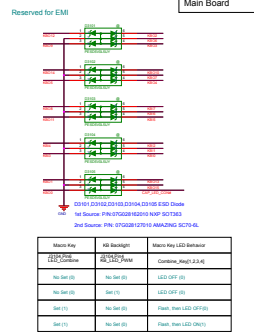
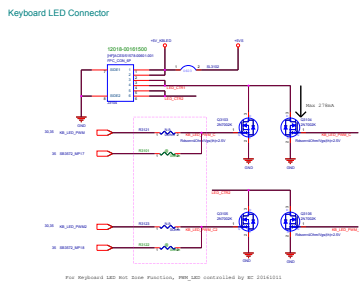
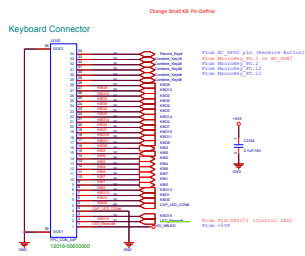


RLD-24



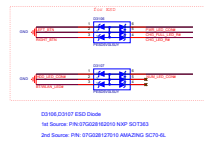
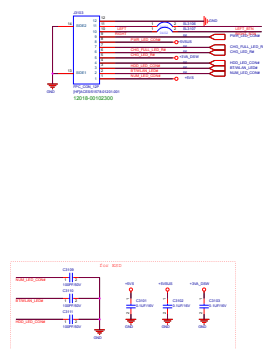
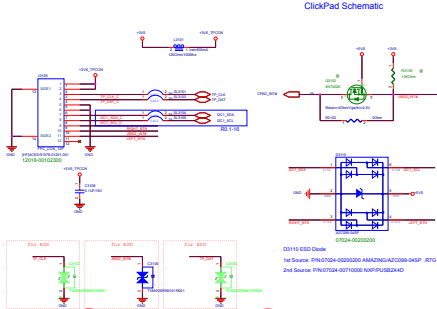
Main Board





To Touchpad

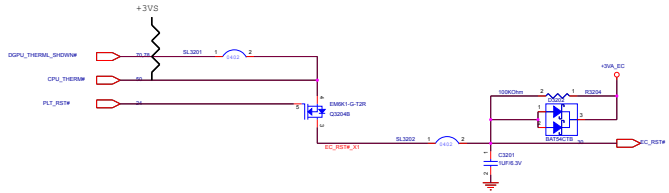
To Touchpad Button



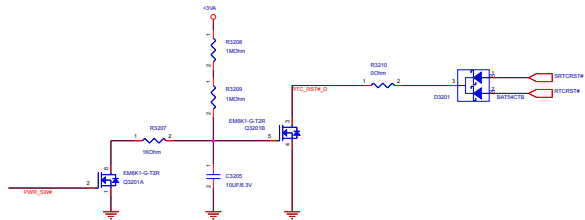
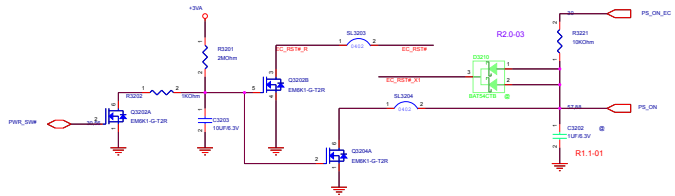
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EC Reset Circuit

Main Board



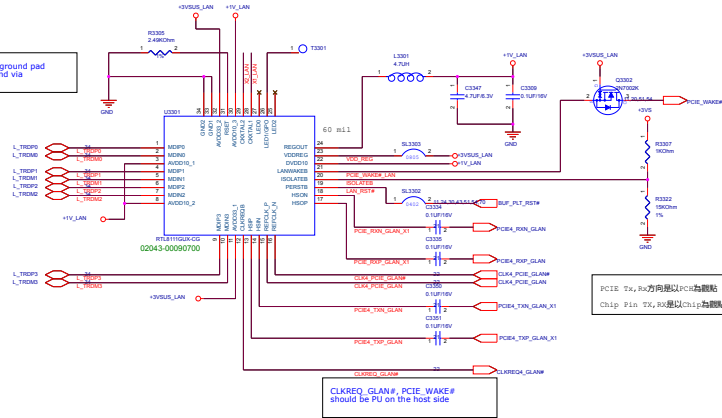
battery embedded (press pwr_sw 10sec, then reset ec)



Main Board

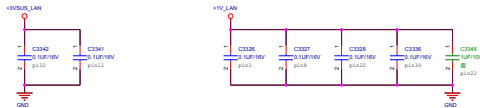
The distance from U3301.24 to L3301 within 200 mil.
The distance from L3301 to C3347 within 200 mil.

33/34 pin ground pad
need ground via

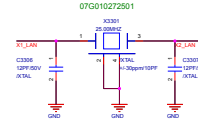


PCIE Tx, Rx 方向是以 PCH 为觀點
Chip Pin TX, RX 是以 Chip 为觀點

CLKREQ_GLAN#, PCIE_WAKE#
should be PU on the host side

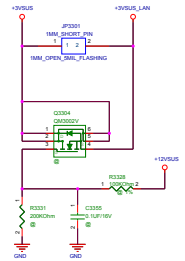


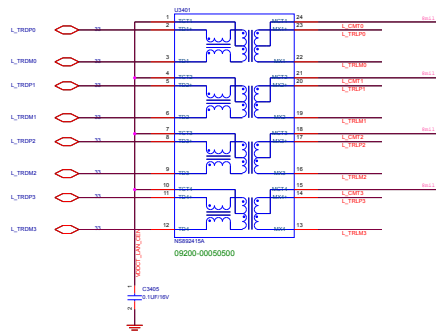
C3348, C3310 close to pin 23 reserved for SWR mode



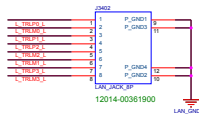
X3301: 25MHZ +/-30ppm/10pF (3225)
1st: P/N:07G010272501 TXC/7V2500001 1
2nd: P/N:07G010952500 HOSONIC/E3FB25

Realtek suggests 3V_LAN raise time >1ms





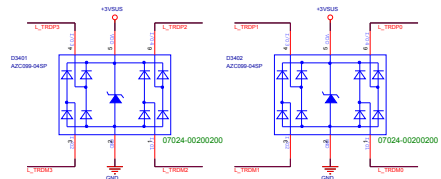
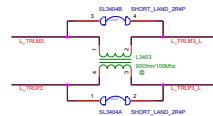
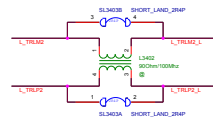
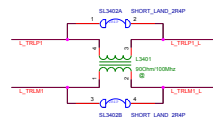
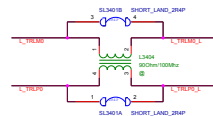
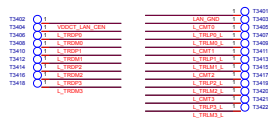
LAN Connector



J3402 LAN Jack

1st Source: P/N:12014-00161700 FOXCONN/JM361 1-NS640003-7H

2nd Source: P/N:12014-00035500 SINGA TRON/2RJ1648-000111F

TEST POINT LAN
Follow Factory ATS test

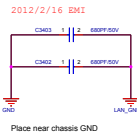
D3401, D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP_R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

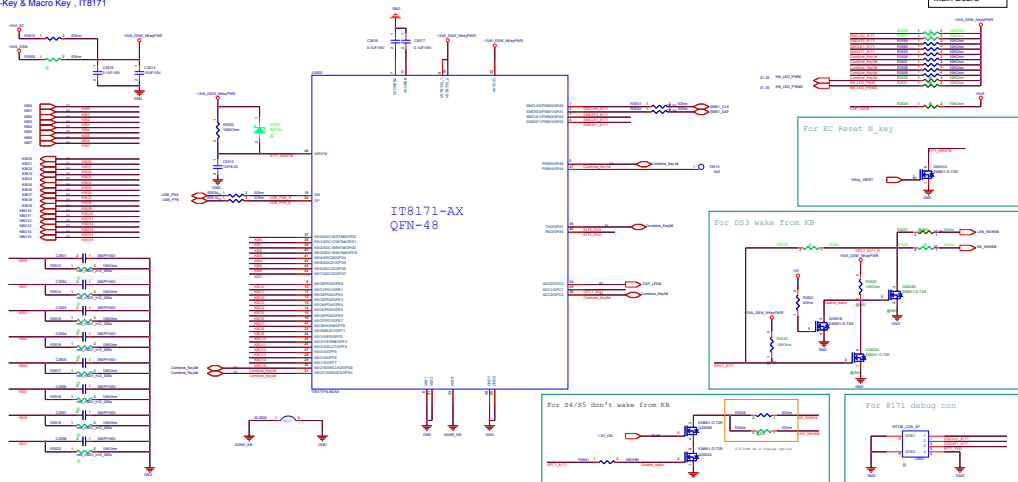


GND_LAN_T 上禁止加任何零件

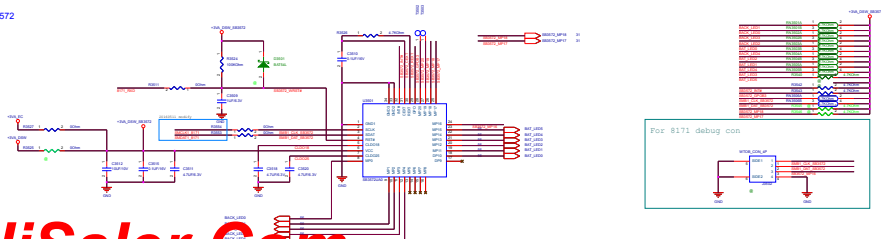


Place near chassis GND

N-Key & Macro Key , IT8171

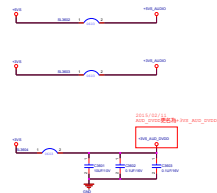
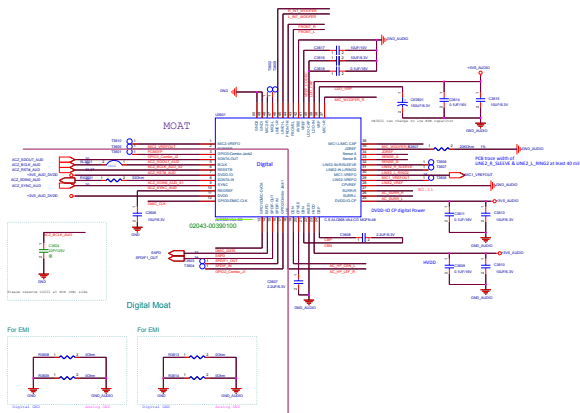


Light Bar , SB3572



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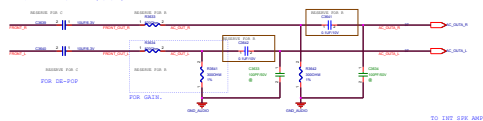
Analog Moat



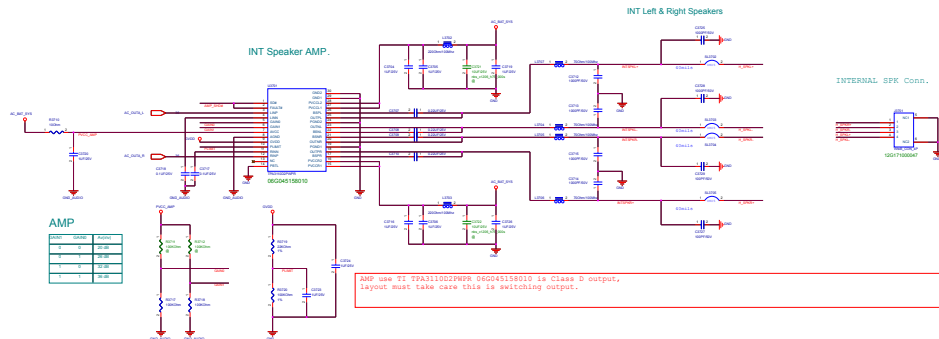
DETECTION



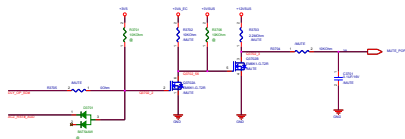
TO INTERNAL SPEAKER (Port-D)



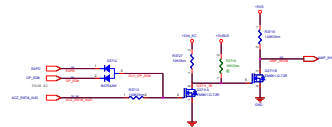
TO INT SPE AMP



EXT JACK MUTE CONTROL



INT SPK MUTE CONTROL



	M 5	M 6	M 7
SPCF IN PLASTIC	LOW	HIGH	LOW
HF IN METAL	LOW	LOW	LOW

The schematic diagram illustrates the HP/SPDIF output stage. It features three DACs (DAC12, DAC13, DAC14) connected to the HP and SPDIF outputs. The circuit includes various resistors (e.g., 100k, 10k, 1k, 100Ω) and capacitors (e.g., 100nF, 10nF, 100pF). A digital control section labeled 'DIGITAL MOAT' contains a 12514-0002-1000 chip. The output is connected to a Port 1 HP/SPDIF connector.

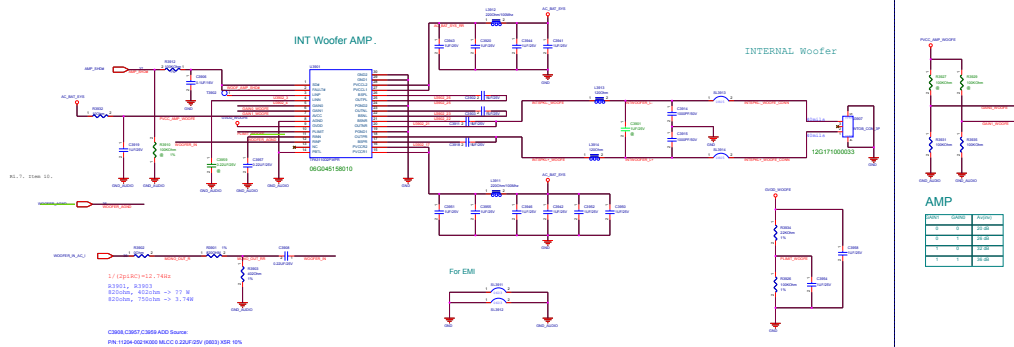
Port 2
EXT MIC/WOOFER

Microphone in Jack

12014-00147500

Port 3
EXT SURR SPK

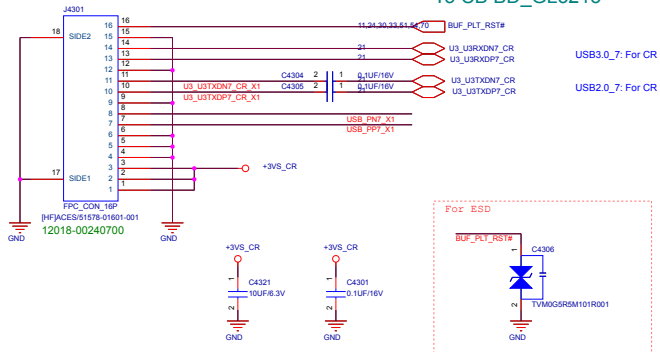
12014-00147500



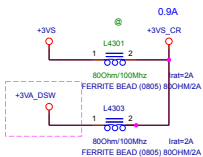
CR I/O Conn. (MB)

Main Board

To CB BD_GL3213

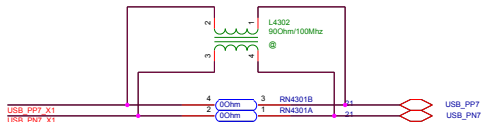


CardReader PWR

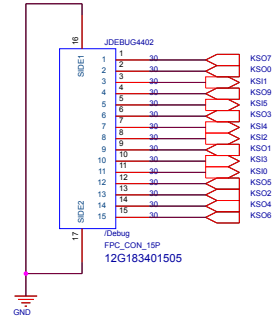
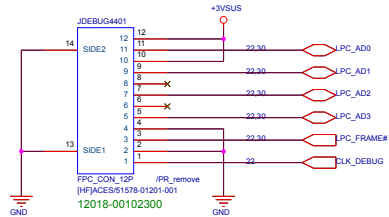


Change to +3VSUS in PR

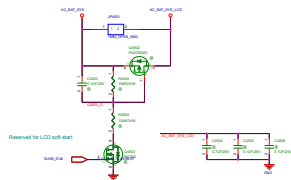
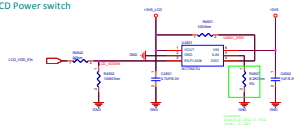
For EMI



LPC Debug Port

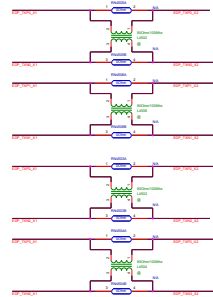


LCD Power switch

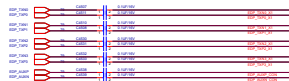


Main Board

For EMI



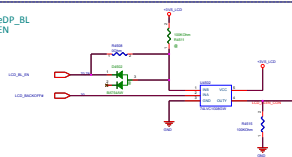
eDP circuit



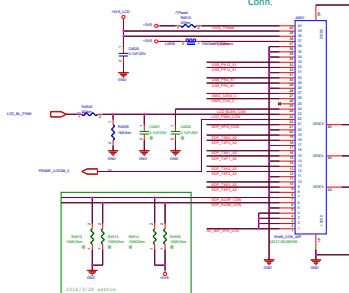
eDP_HPD



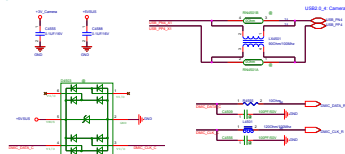
eDP_BL EN



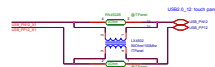
eDP Panel Conn.

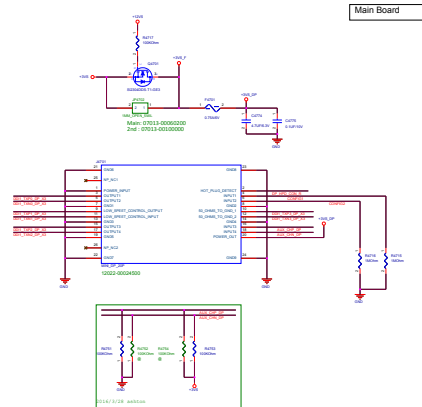
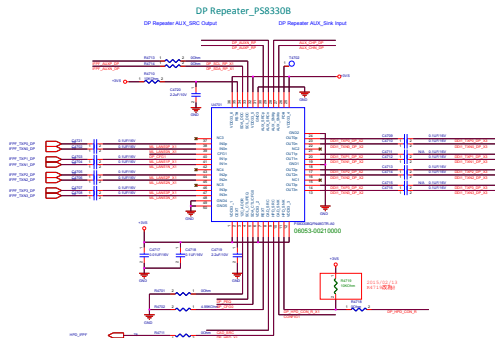


Camera & D-MIC

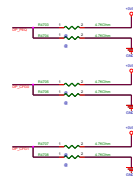
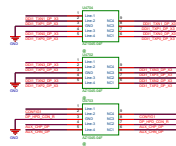
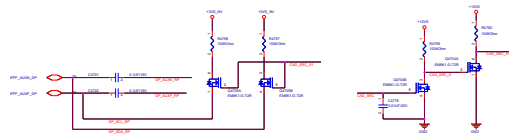


Touch Panel

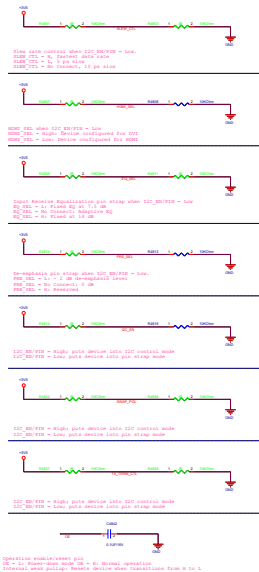




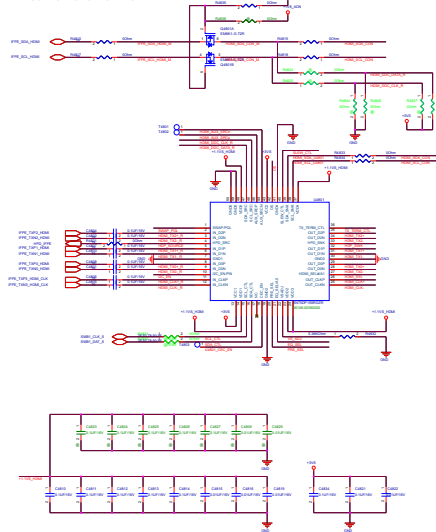
2014/3/28
 BULTEK AL-5.00 reference Purusa Design Circuit P583308
 Via WinCEP To HMC Double No Display Issue



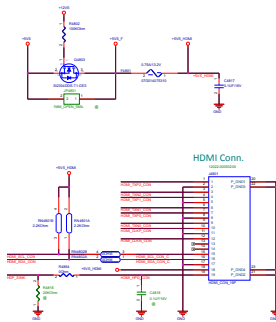
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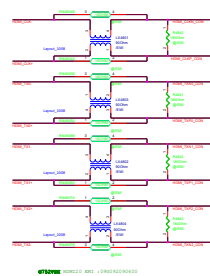
HDMI Active-Level Shift



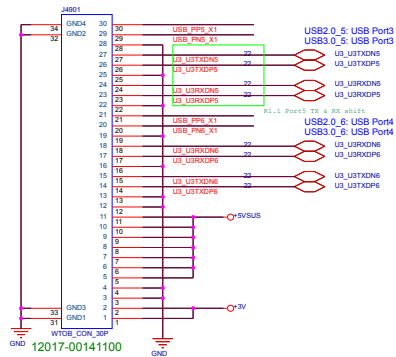
HDMI PWR_+5VS_HDMI



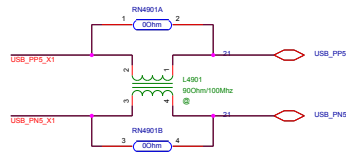
HDMI EMI



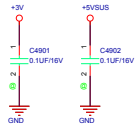
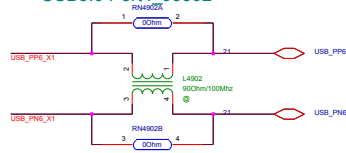
To USB3.0 I/O Board (PAGE55)



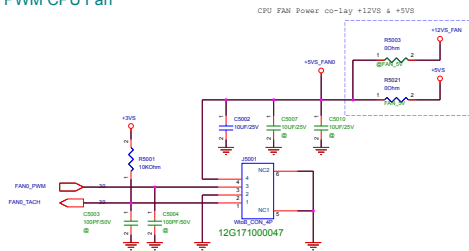
USB3.0 Port3_J5501



USB3.0 Port4_J5502

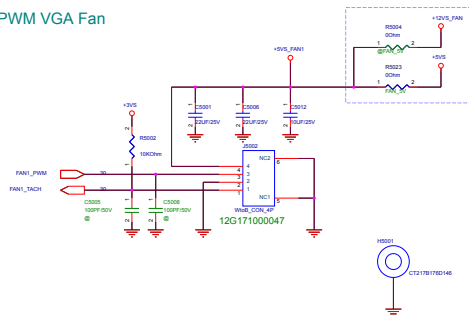


PWM CPU Fan

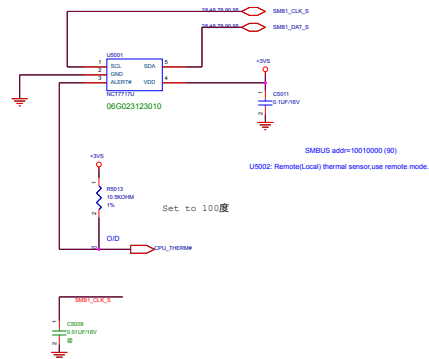


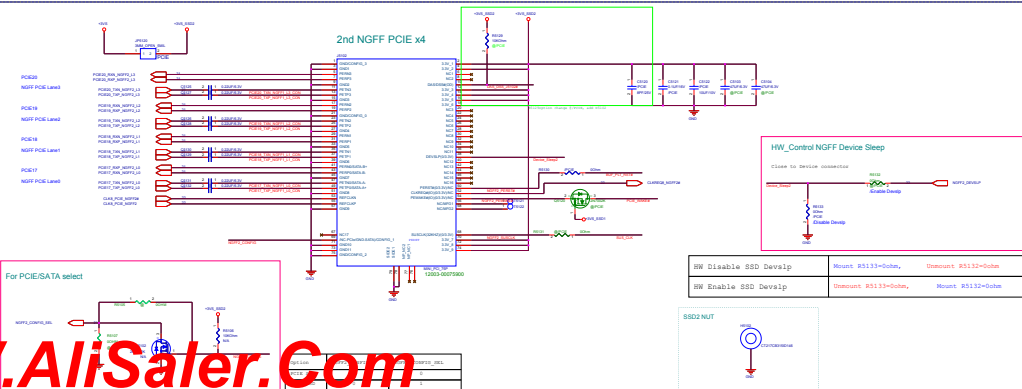
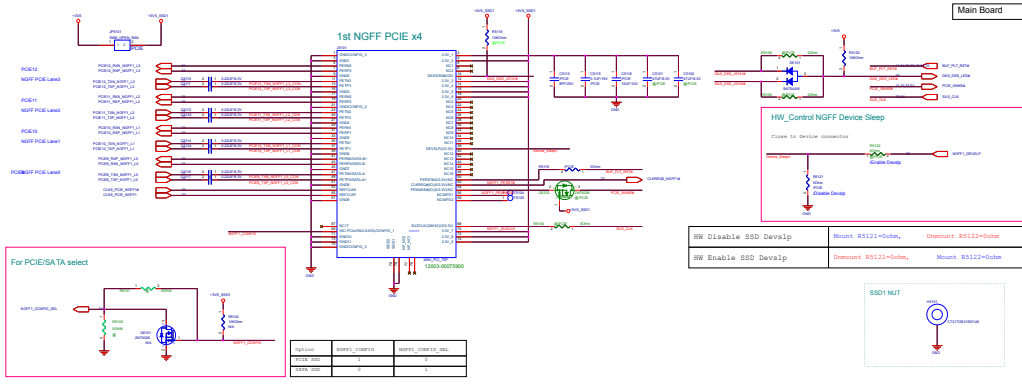
GPU FAN Power co-lay +12VS & +5VS

PWM VGA Fan



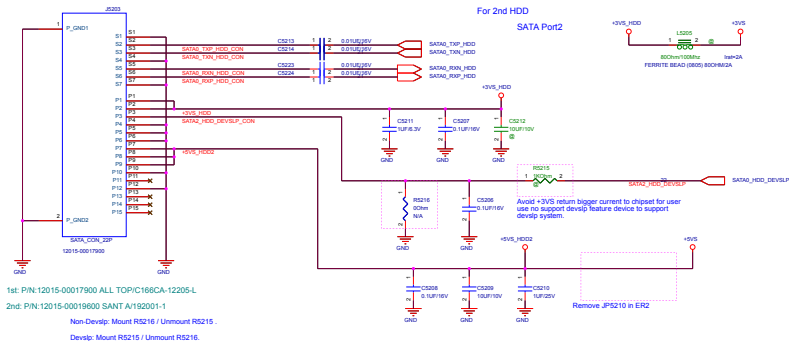
CPU Thermal Sensor





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2nd HDD



EMI Request



1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F

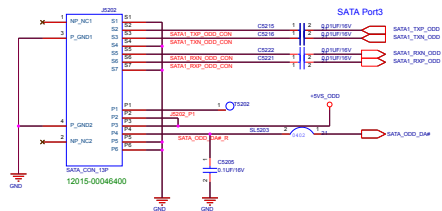
2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

For RF requirement

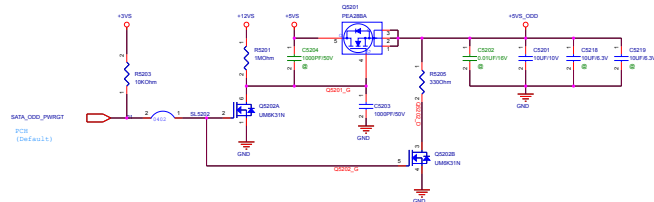
EMI Request0520



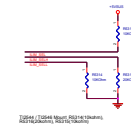
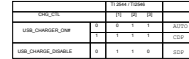
ODD



ODD Power

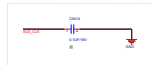
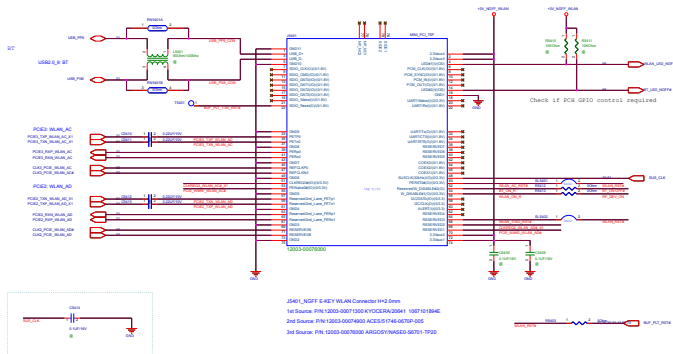


Main Board



2nd Source: PIN:07024-00710000 NXP/PU5B2X4D

NGFF M.2 TYPE_E-KEY WIFI

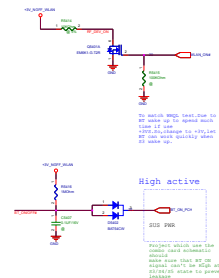


J5401_NGFF E-KEY WLAN Connector H=2.5mm
1st Source: P/N:12003-00071300 KYOCERA/20641 1067101894E
2nd Source: P/N:12003-00074900 ACES/51746-0670P-005
3rd Source: P/N:12003-00070000 ARGOSY/NA50-56701-1P20

4th Source: P.91-12003-00022-000 JAC:SM37505712-5AC

[illegible]

WLAN & BT ON



WLAN NUT

PRGGE:

ST 21 07 17 00 46
13GNB210M025-1

LOCAN WLAN CARD NUT
wlan_nut_240

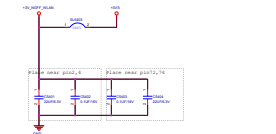
CHASS

For EMI

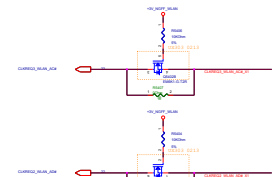
Reserve for post noise

Diagram illustrating a circuit for EMI suppression. It shows a power line (Main Power) connected to a diode (C4508) and a capacitor (C4509, 0.1uF/10V) in parallel, both connected to ground (GND). The text "Reserve for post noise" is written above the capacitor branch.

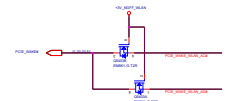
WLAN PWR_+3V_NGFF_WLAN
(Non-ISCT)



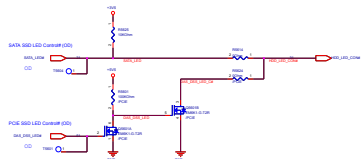
WLAN CLKREQ#



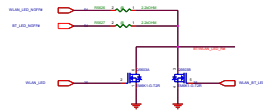
WLAN_Wake# Control



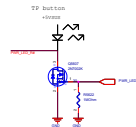
HDD LED & PCIE SSD LED



BT/WLAN LED Control

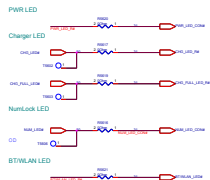


PWR LED Control



Main Board

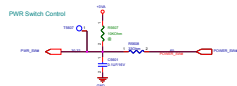
To TP Button CONN



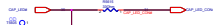
OS LED Control



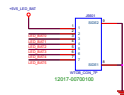
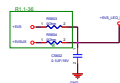
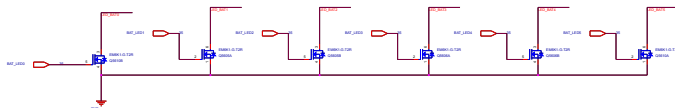
To Power Button IO BD



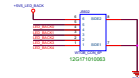
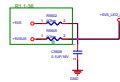
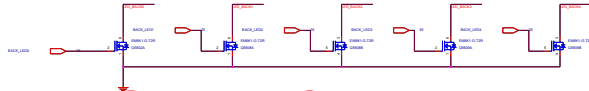
To Keyboard CONN CapsLock LED



To LED BAT BAR

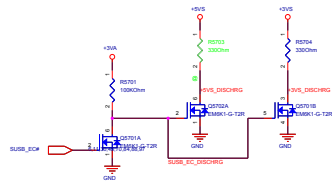


To LED BACK BAR

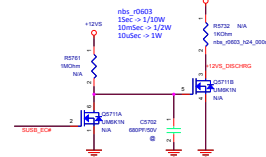
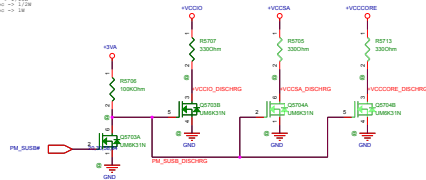


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Main Board



sta_r0403
15mV -> 1/10W
10mSec -> 1/2W
10uSec -> 1W

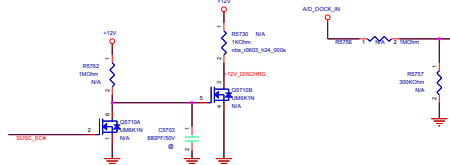
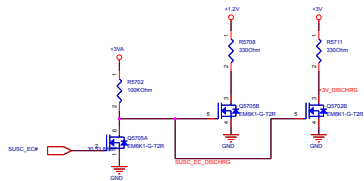


nbs_r0603
15mV -> 1/10W
10mSec -> 1/2W
10uSec -> 1W

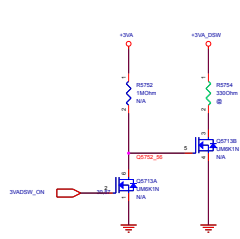
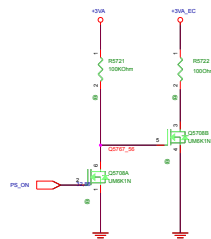
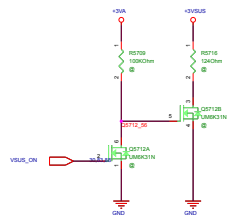
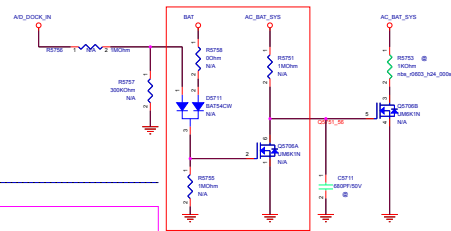
+12V & +12V5 需轉解+12V500B Load switch 應才能啟動

sta_r0403
15mV -> 1/10W
10mSec -> 1/2W
10uSec -> 1W

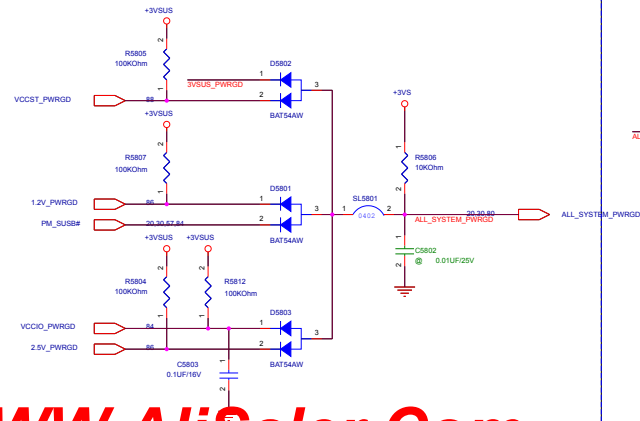
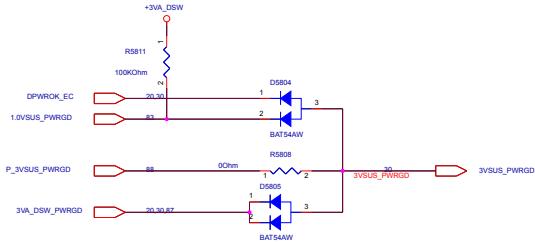
SUSC_EC# turn off discharge before +12V ON
+12V turn on discharge after SUSC_EC# OFF



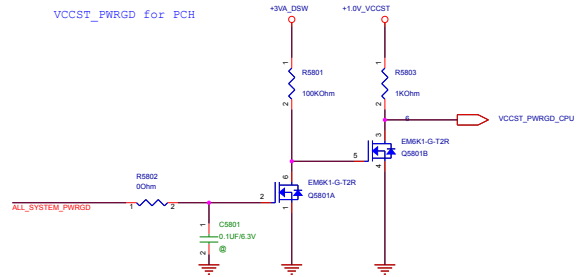
每小時耗 0.45mW
每個月耗 324mW
0.45mW=(15X15/1M)x2



Main Board



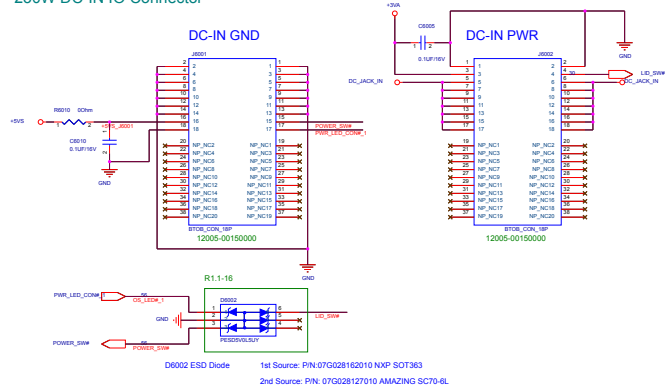
VCCST_PWRGD for PCH



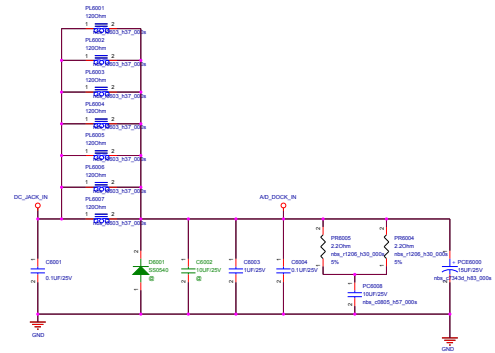
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ASUS		Project Name	Rev
C752VSK			R2.0
Title : PRO Protect			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: Ashton yang
Custom			
Date: Wednesday, October 12, 2016	Sheet	58	of 102

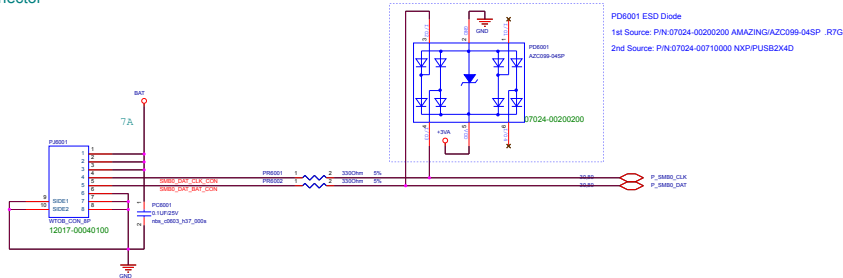
230W DC-IN IO Connector



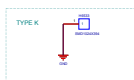
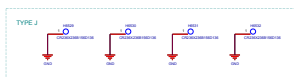
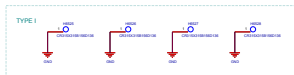
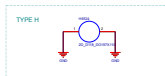
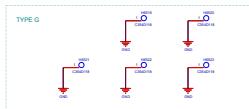
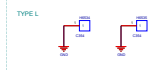
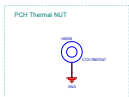
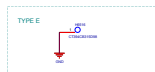
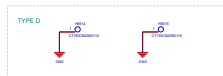
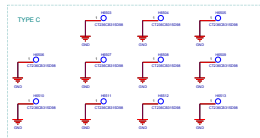
Main Board



Battery Connector



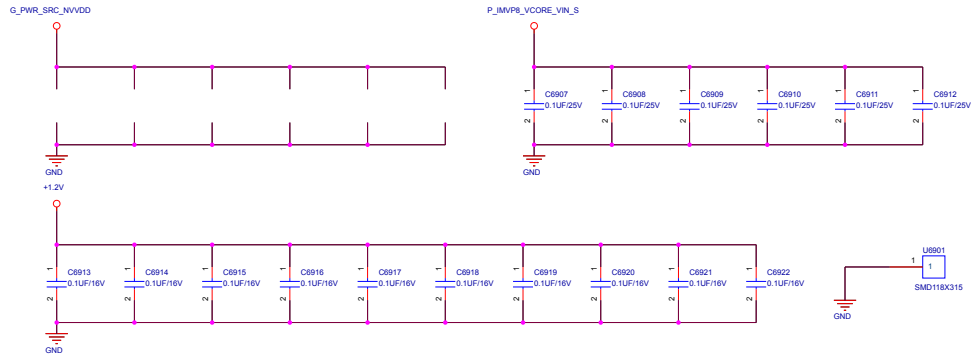
TOP Component

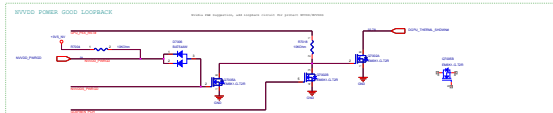


Main Board

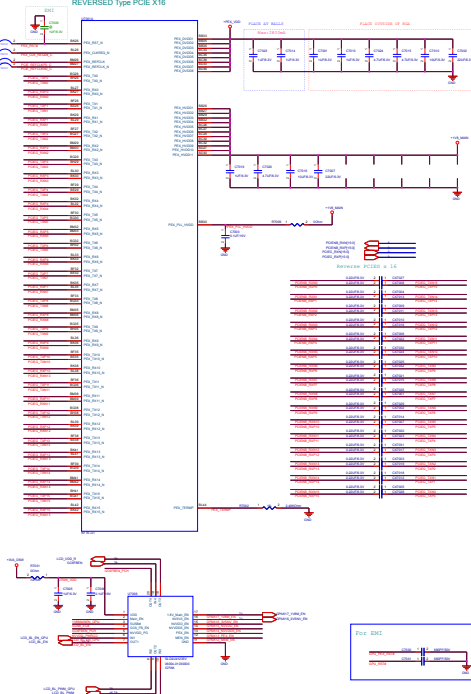
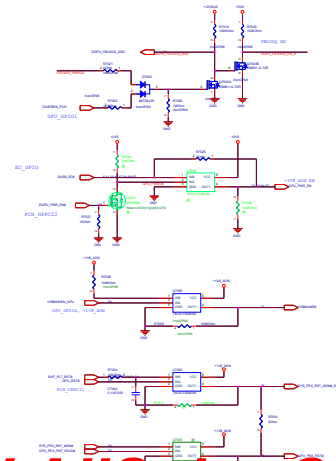
BOT Component

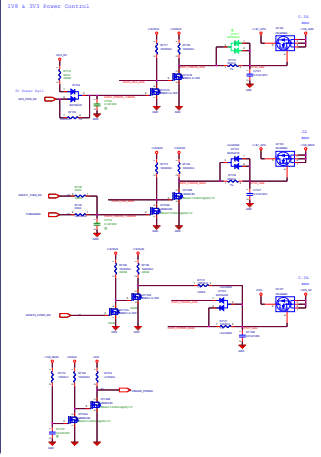
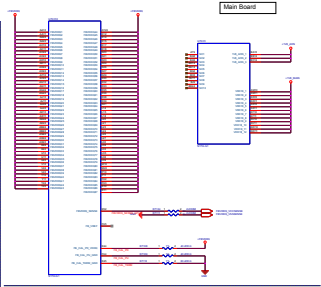
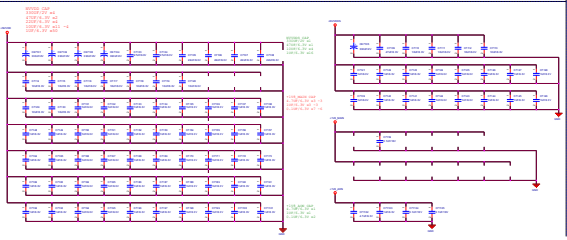
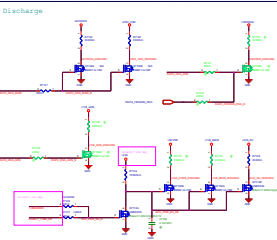
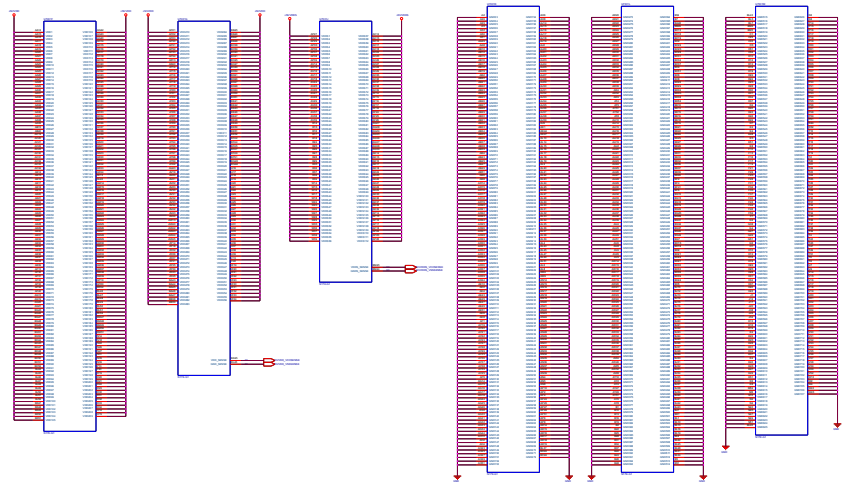
EMI

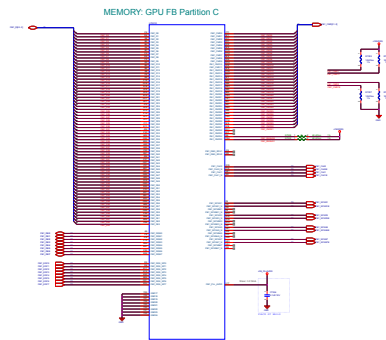
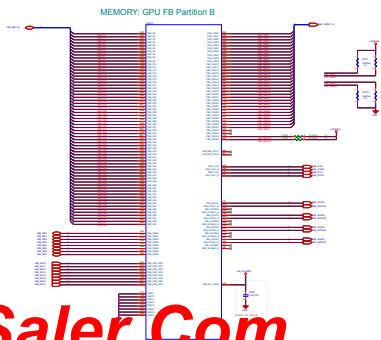
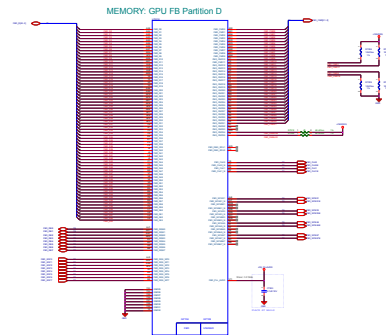
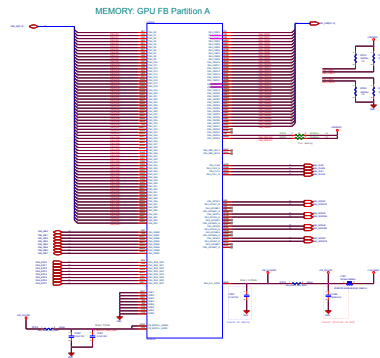




GPU POWER SEQUENCE CONTROL



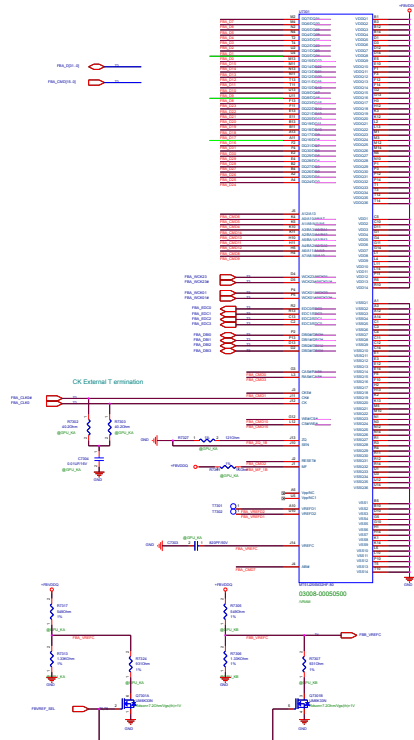




Memory Bank

FBA Partition Memory (1 of 2)

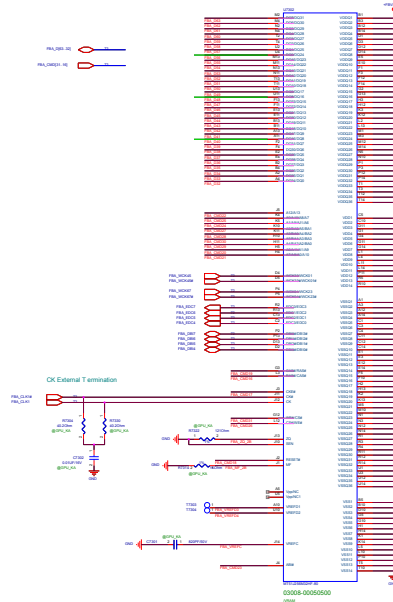
MF=1 Mirror



FBA Partition Memory (2 of 2)

Main Board

MF=0 Normal



01 3-02 01 2-02

USE GDS5 VMM (2886 x 32 (512MB))

1st PIN 03008-00030100 HYNNH5GC41Q4MR9-T2C (M-dw) .Step: 0 x2

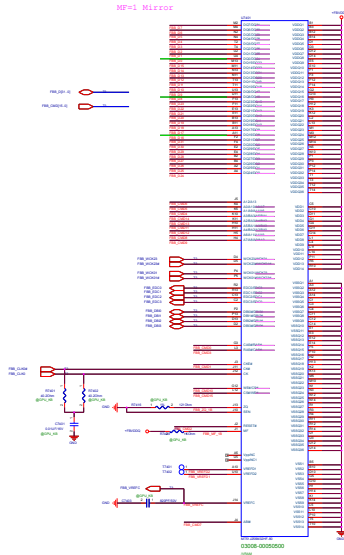
2nd PIN 03008-00030200 SAMSUNGK4K4132DF-HC33 .Step: 0x3

3rd PIN 03008-00030400 MicronEDW532BAG-60 F (B-dw) .Step: 0x4

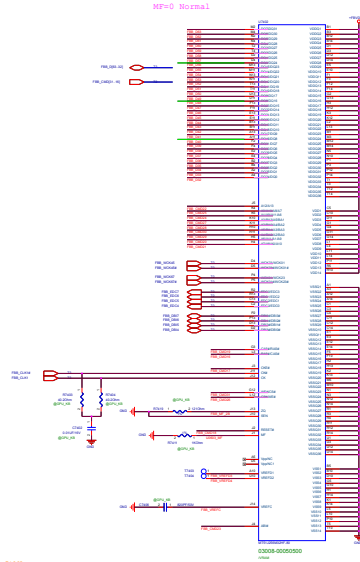
GDS5 MODE SELECTION

Mode	MF	MF1	MF2
00	0	0	0
01	1	0	0
02	0	1	0
03	1	1	0
04	0	0	1
05	1	0	1
06	0	1	1
07	1	1	1

FBB Partition Memory (1 of 2)



FBB Partition Memory (2 of 2)



03-000 03-000

03008-00050000 HYPERMAGNETIC T3C (8-10-10) (8-10-10)

1st PIN: 03008-00050000 HYPERMAGNETIC T3C (8-10-10) (8-10-10)

2nd PIN: 03008-00050000 HYPERMAGNETIC T3C (8-10-10) (8-10-10)

3rd PIN: 03008-00050000 HYPERMAGNETIC T3C (8-10-10) (8-10-10)

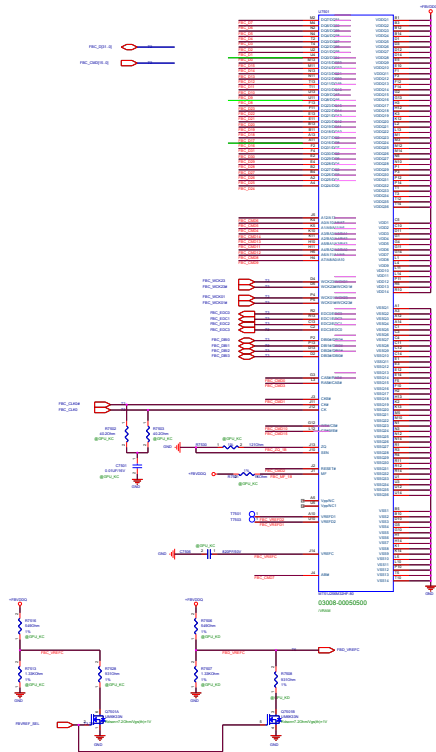
GDD5 MODE SELECTION

MODE	MF	MODE	MODE
1st	0	1st	0
2nd	0	2nd	0
3rd	0	3rd	0

Main Board

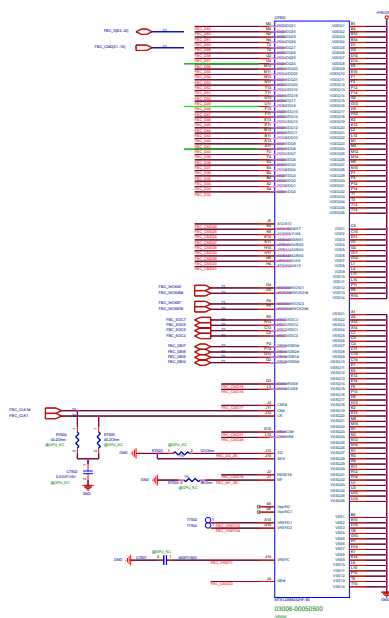
FBC Partition Memory (1 of 2)

MF=1 Mirror



FBC Partition Memory (2 of 2)

MF=0 Normal



PH 3-00 PH 3-05

USE GDDR5 VRAM (2GB x 32 (128MB))

1st PIN 0308-00030100 HYUNDAI H5GQ4H4MTR-T2C (M-die) (Strap 0 x2)

2nd PIN 0308-00030200 SAMSUNG K4G41322FC HCCS (Strap 0x3)

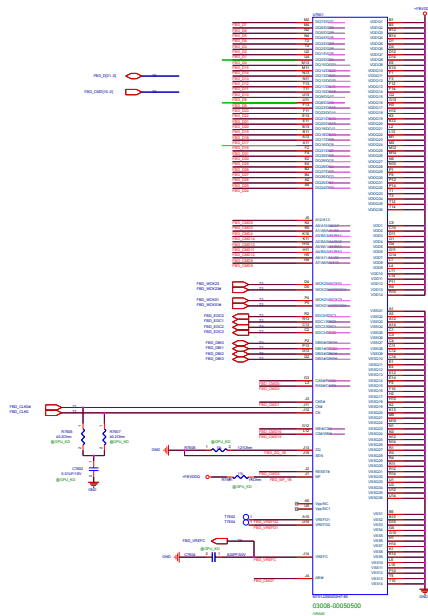
3rd PIN 0308-00030400 Micron EDVH432BAG-60-P (B-die) (Strap 0x4)

GDDR5 MODE SELECTION

MODE	MF	MODE	MODE
0	0	0	0
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15
16	16	16	16
17	17	17	17
18	18	18	18
19	19	19	19
20	20	20	20
21	21	21	21
22	22	22	22
23	23	23	23
24	24	24	24
25	25	25	25
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27	27	27	27
28	28	28	28
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31	31	31	31
32	32	32	32
33	33	33	33
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89	89	89	89
90	90	90	90
91	91	91	91
92	92	92	92
93	93	93	93
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95	95	95	95
96	96	96	96
97	97	97	97
98	98	98	98
99	99	99	99

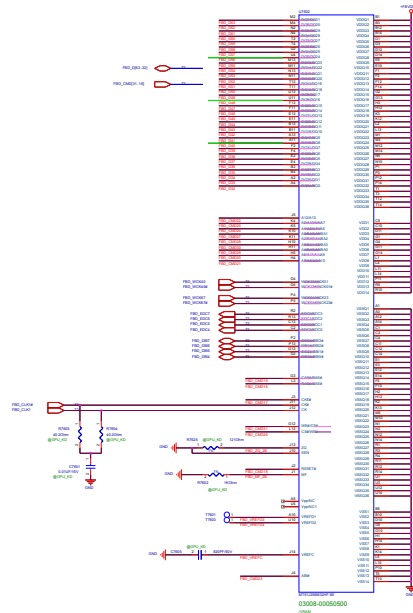
FBD Partition Memory (1 of 2)

MF=1 Mirror



FBD Partition Memory (2 of 2)

MF=0 Normal



R1.3-02 R1.2-25

USE GDDR5 VRAM (28Mb x 32 (512Mb))

1st: P/N:03008-00030100 HYNIXH5GC4H24MFR-T2C (M-die) ,Strap: 0 x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

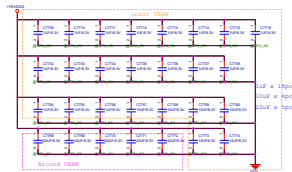
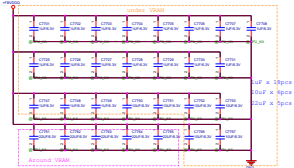
3rd: P/N:03008-00030400 Micron/EDW4032BAG-60-F (B-die) ,Strap: Oak

GDD5 MODE SELECTION

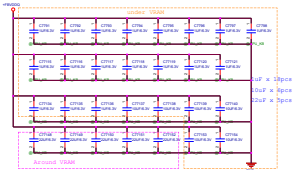
Model	df	SS	MS
1	1	1	1.000
2	1	1.000	1.000
3	1	1.000	1.000
4	1	1.000	1.000

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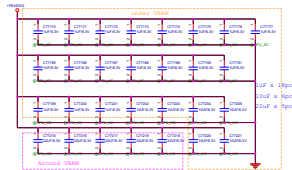
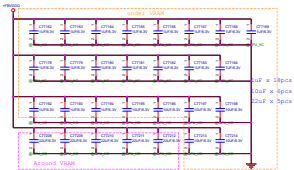
Channel A



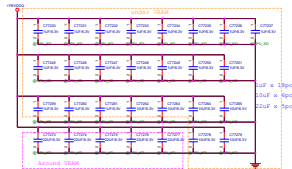
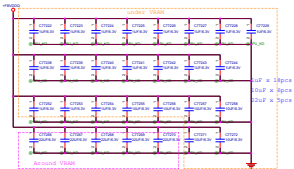
Channel B



Channel C

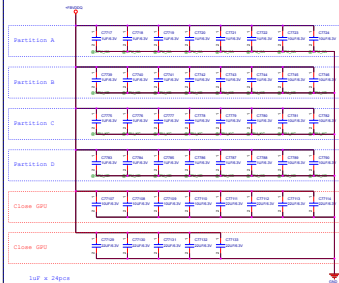


Channel D

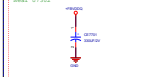


VRAM_FWR_FBVDQ

Main Board



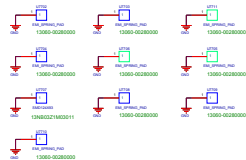
Wear U7302

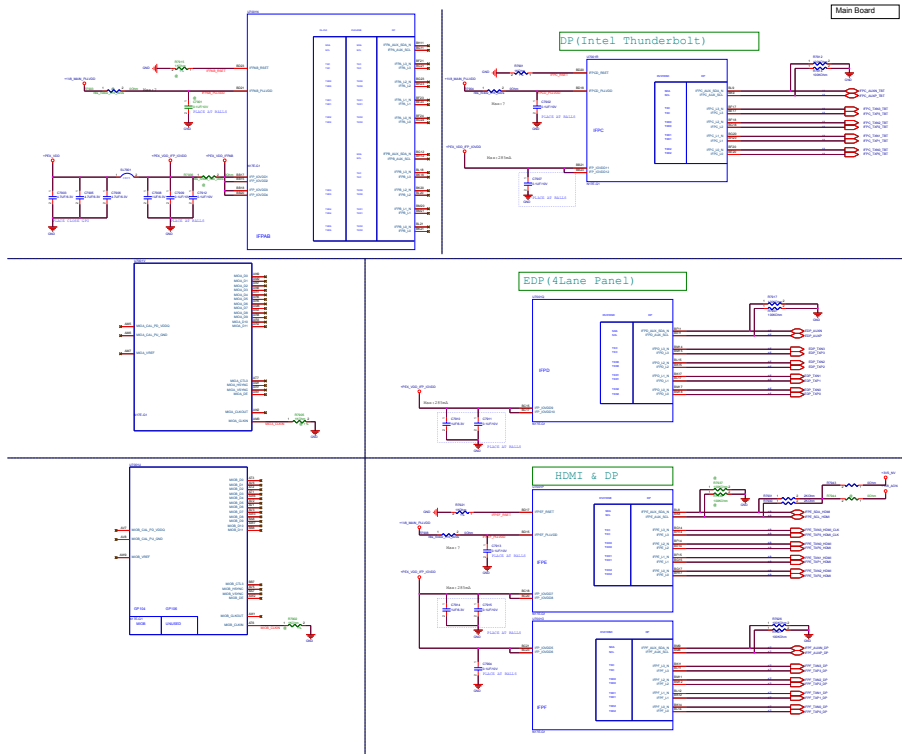


DGPU EMI GND Pad

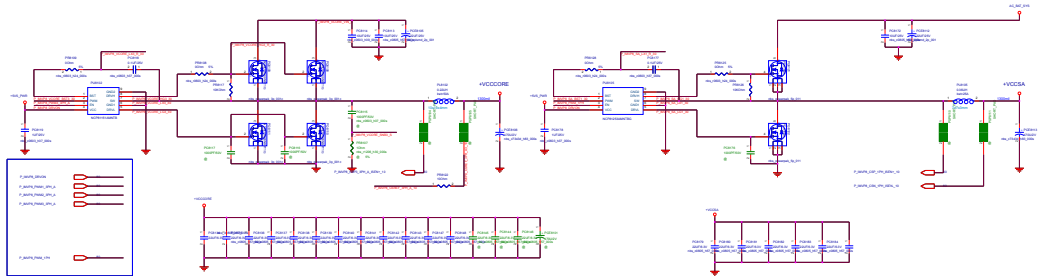
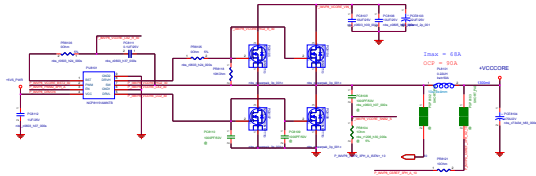
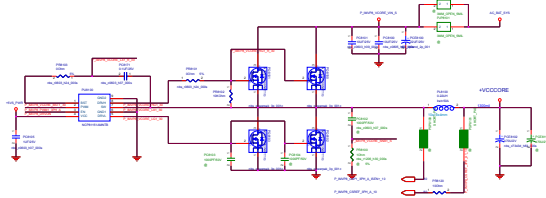
EMI

EMI DGPU Spring

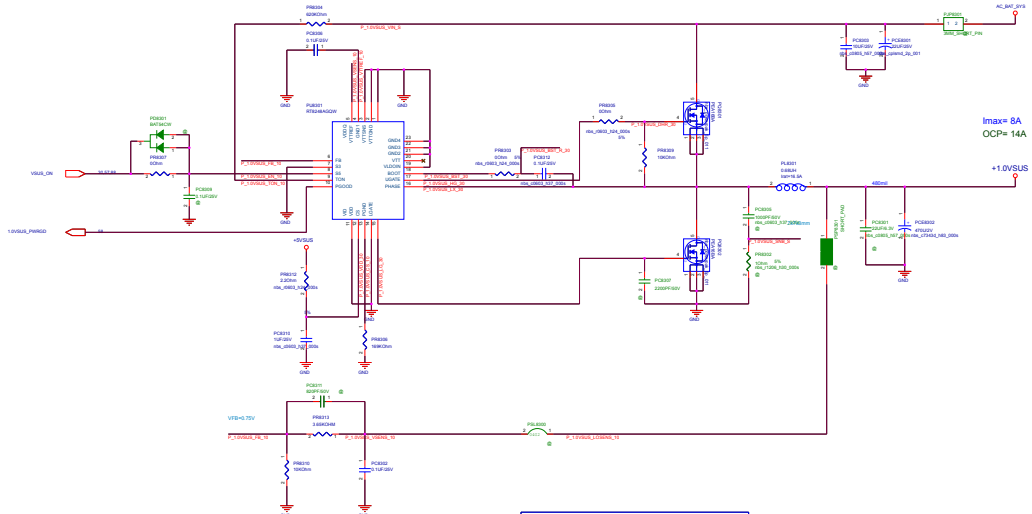




Skylake IMVP8 Power [For CPU]

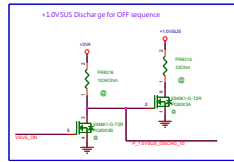


+1.0VSUS [For PCH]



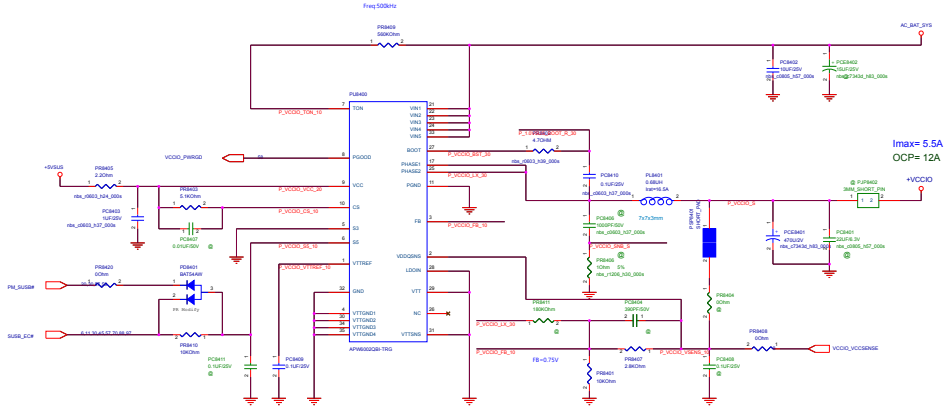
I_{max} = 8A
OCP = 14A

+1.0VSUS



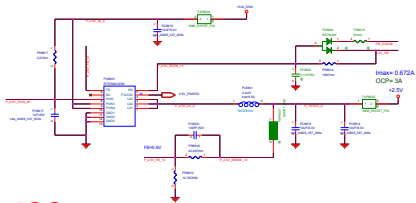
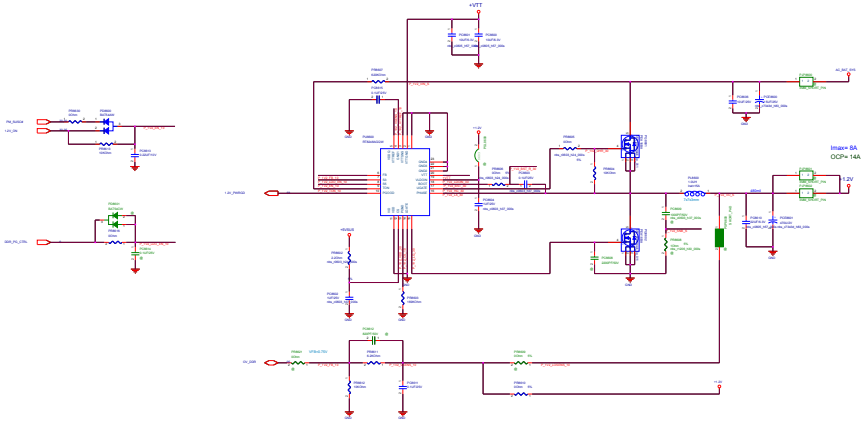
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+VCCIO [For CPU]



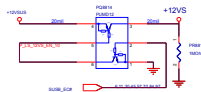
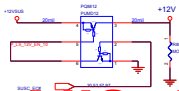
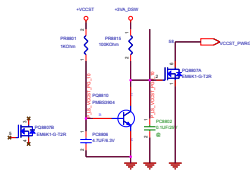
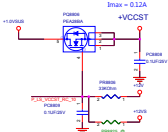
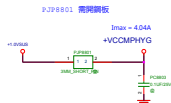
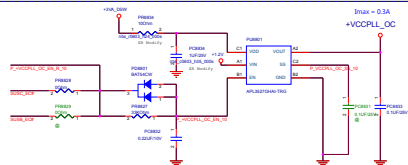
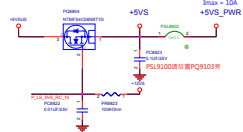
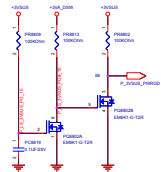
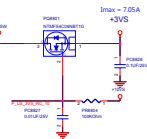
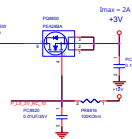
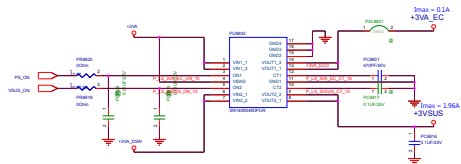
«Core Design»

+1.2V / VTT / 2.5V[For Memory]



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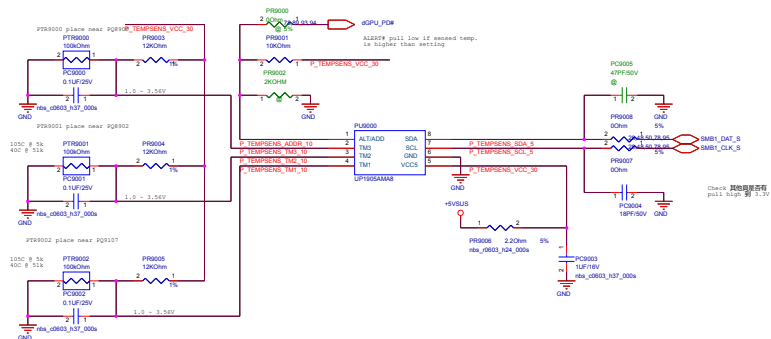
Main Board



Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR0001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR0002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

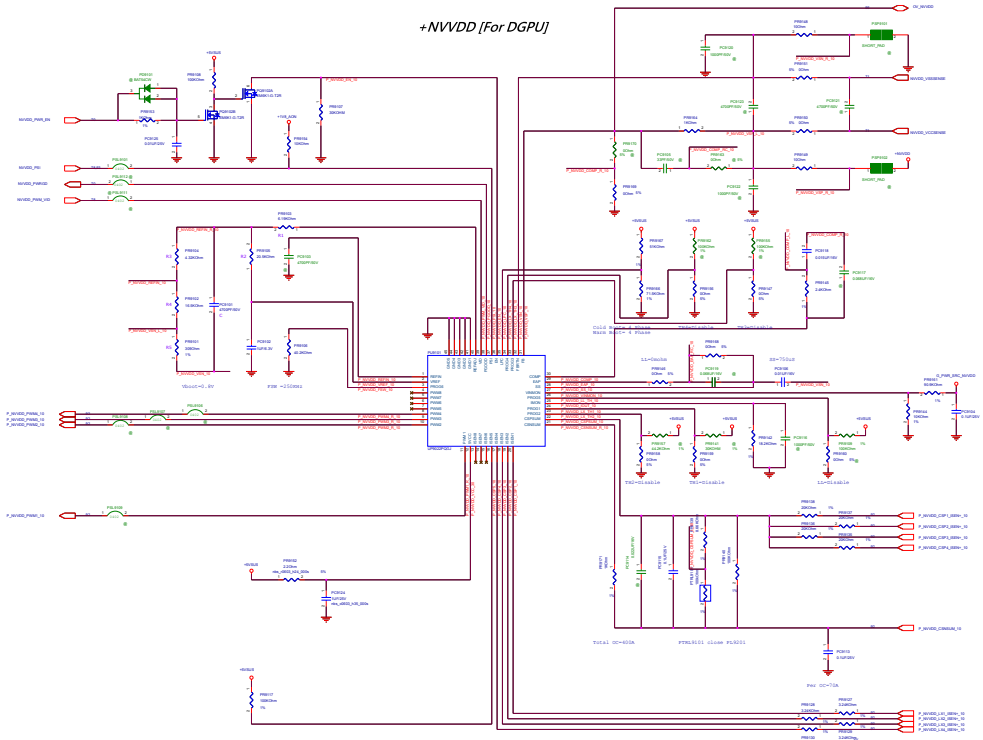
Address	Gx05	Gx01	Gx02	Gx03	Gx04	Gx05	Gx06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

Main Board

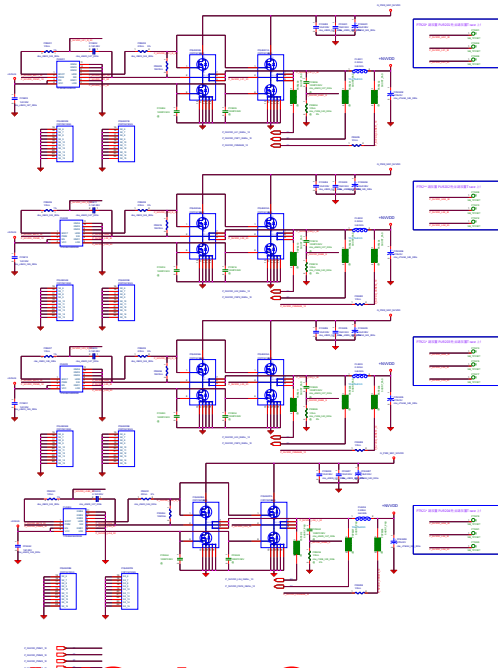


		Project Name C752VSK		Rev R2.0
Title : PW_PROTECTION				
Size	Dept.: NS Power team		Engineer: Benson Hsu	
AA				
Date: Wednesday, October 12, 2016	Sheet		90	of 102

+NVVDD [For DGPU]

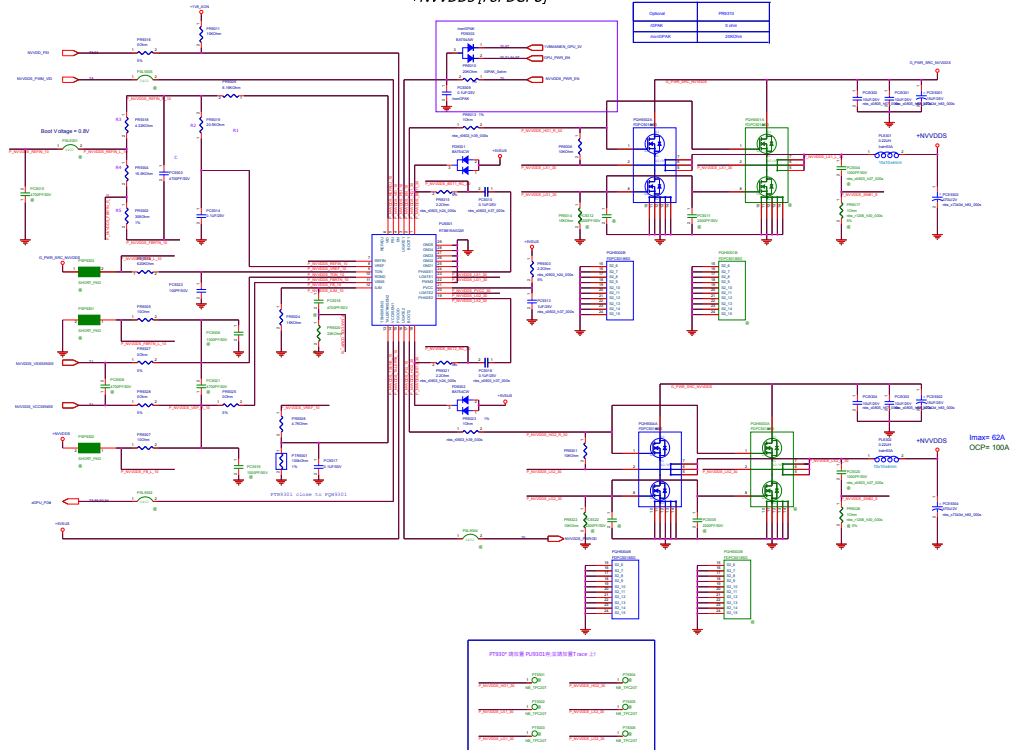


+NVVDD [For DGPU]



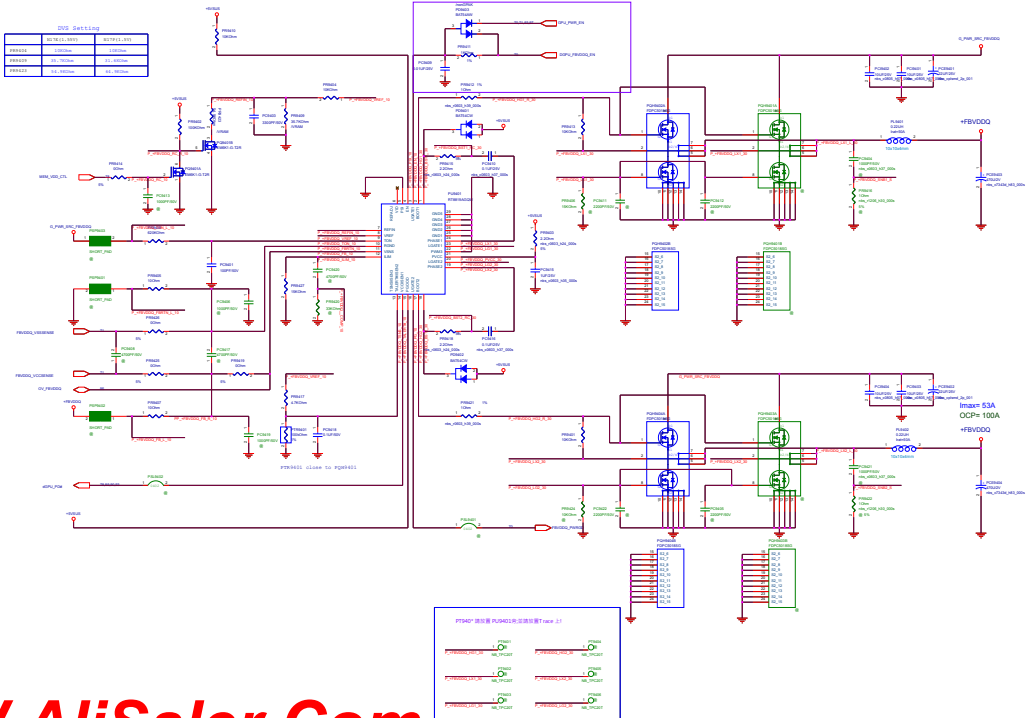
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+NVVDD5 [For DGPU]

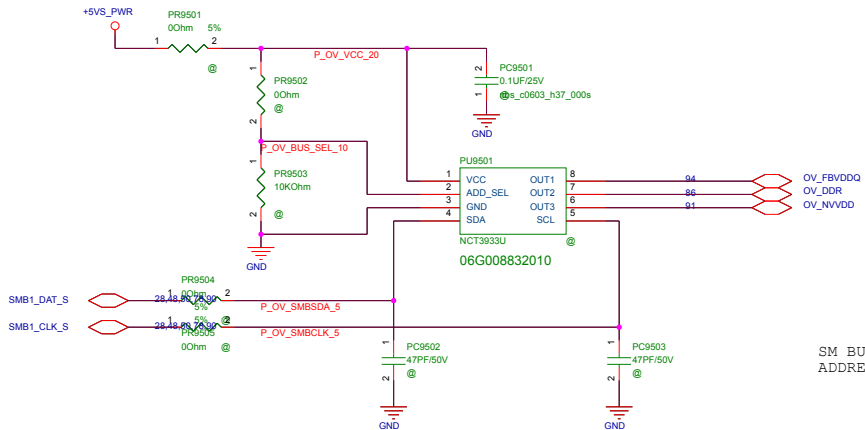


+FBVDDQ [For VRAM]

	8019E (1.00W)	8019P (1.00W)
FR0004	1.0000um	1.0000um
FR0005	35.7000um	32.6000um
FR0023	0.4.9000um	0.6.9000um




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SM BUS SLAVE
ADDRESS:0X2A

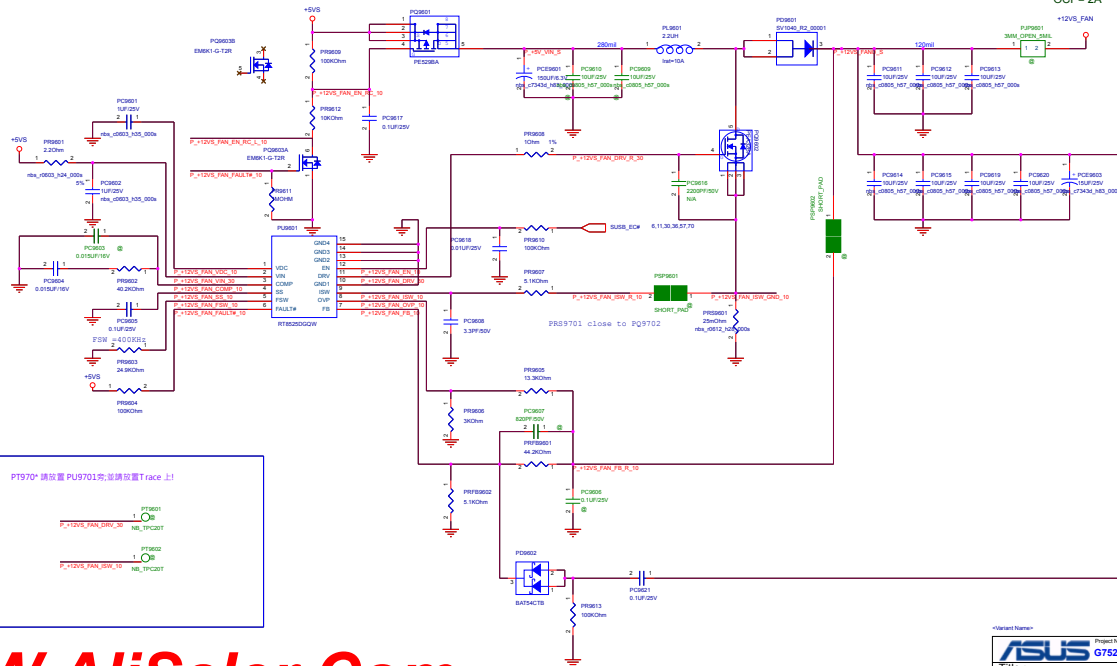
<Core Design>

		Project Name		Rev
		G752VSK		R2.0
Title : PW_OV				
Size	Dept.:		Engineer:	
A	NB Power team		Benson	
Date: Wednesday, October 12, 2016			Sheet	95 of 102

I_{max} = 1.5A

OCP = 2A

+12V_{S_FAN}

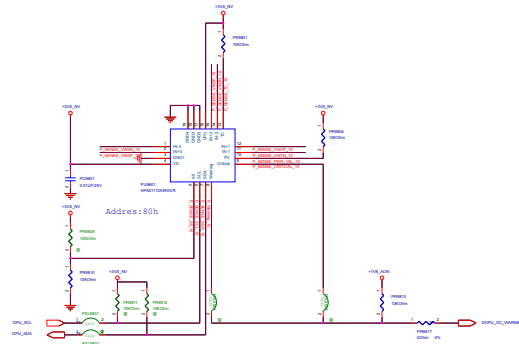
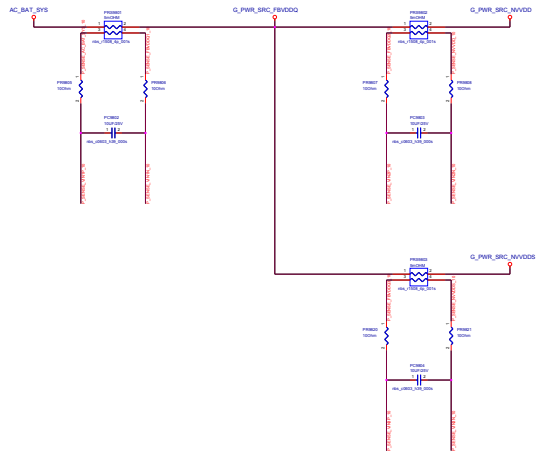


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<Variant Name>

Project Name		Rev
ASUS G752VSK		B2.0
Title : PW_+12V _{S_FAN}		
Size	Dept. : NB Power team	Engineer : Benson
Date : Wednesday, October 13, 2016		
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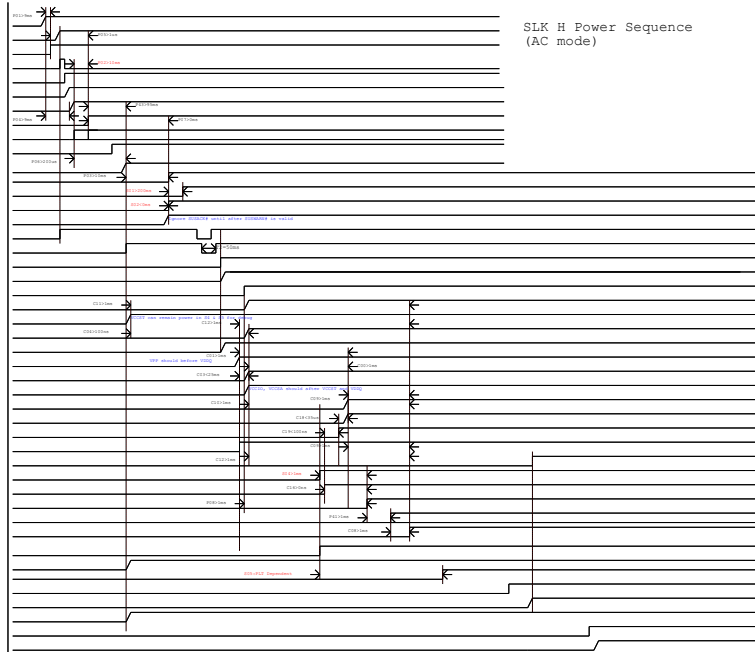




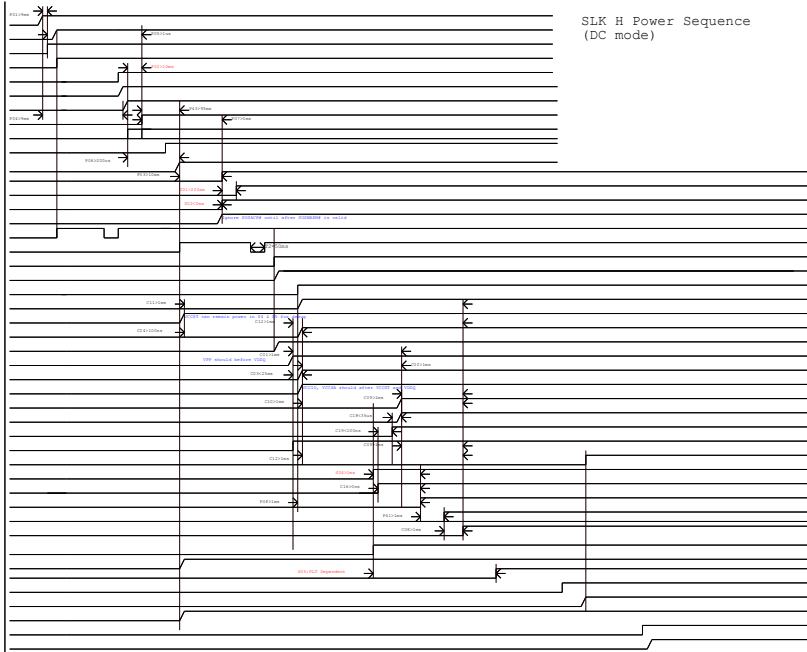


AC-IN Mode

C:CPU (+PFCBATT)+30A_RTC
 P:PCW (AC_BAT_STS)+30A/+30A
 S:PLT (+30A_RTC)+PFCBATT (PCR)
 Power (Power)AC_IN_OCH (EC)
 Signal (EC)PS_ON(+30A_EC)
 (PS_ON)+30A_EC (EC)
 (30A200M_ON)+30A_DSW (30A_DSW_PNRGD)
 (EC)DPNROK_EC (PCR)
 (+30A_DSW)PM_BATLOM (PCR)
 (PCR)PM_SLP_S0S# (EC)
 (VDSO_ON)+1.0VDSO_VCCPWRM(1.0VDSO_PNRGD)
 (EC)PM_BSMRST#_PCR (PCR)
 (PCR)SUSWRAR# (EC)
 (EC)ME_AC_PRESENT_PCH (PCR)
 (EC)PCH_SUSACK# (PCR)
 (PWR_Switch)PWR_DSW (EC)
 (EC)PM_PWRSTN# (PCR)
 (EC)S0SC_ECH (Power)
 (S0SC_ECH)+1.2V/+5V/+3V
 (EC)S0SB_ECH (Power)
 (S0SB_ECH)+1.2V/+5V/+3V
 (VDSO_ON)+1.0V_VCCST_VCCPLL (VCCST_PNRGD)
 (+VCCIO)+VCCSTO
 (1.2V_ON)+2.5V(2.5V_PNRGD)
 (1.2V_ON)+VDSO_CPU(1.2V_PNRGD)
 (+1.2V)+VCCPLL_OC
 (S0SB_ECH)+VCCIO (VCCIO_PNRGD)
 (ALL_SYSTEM_PNRGD)+VCCSA (IMVPS_PNRGD)
 (DDR_VTT_CTRL)+0.6V
 (CPU)DDR_VTT_CTRL (Power)
 (Power)1.2V_PNRGD (AMD)
 (Power)IMVPS_PNRGD
 (AMD)ALL_SYSTEM_PNRGD (CPU/PCR/EC/Power)
 (ALL_SYSTEM_PNRGD)+VCCST_PNRGD_CPU (CPU)
 (EC)PM_PNRGD_PCH (PCR)
 (PCR)CLK_PCH_CLK (CPU)
 (PCR)H_CPU_PNRGD (CPU)
 (ALL_SYSTEM_PNRGD)P_IMVPS_E0 (Power)
 (CPU)P_S0TD_DATA_K2 (Power)
 (EC)PM_STS_PNRGD_PCH (PCR)
 (PCR)PLT_RST# (CPU/EC/Device)
 (P_IMVPS_DRV0)+VCCOCORE (IMVPS_PNRGD)
 (CPU)H_THERMSTRIP (PCR)
 (PCR)DDR4_DRAMRST# (Memory)
 +VCCGT



SLK H Power Sequence (AC mode)

[illegible]SLK H Power Sequence
(DC mode)